

# ER-OLEDM2002-1 Series

## OLED Display Datasheet



## EastRising Technology Co., Limited

**Attention:**

- A. Some specifications of IC are not listed in this datasheet. Please refer to the IC datasheet for more details.
- B. The related documents for interfacing, demo code, ic datasheet are all available, please download from [www.buydisplay.com](http://www.buydisplay.com).
- C. Please pay more attention to "Quality Control" in this Datasheet. We assume you already agree with these criterions when you place an order with us. No more recommendations.

REV	DESCRIPTION	RELEASE DATE
1.0	Preliminary Release	Jul-02-2011

## ORDERING INFORMATION

Order Number

Part Number(Order Number)	Description
ER-OLEDM2002-1Y	20x2 Character OLED Display with Adaptor Board in Yellow Color
ER-DBOM2002-1	Testing or Demo Board ER-OLEDM2002-1 Series Products

Image



↑ ER-OLED2002-1Y

## 1. Module Basic Specification

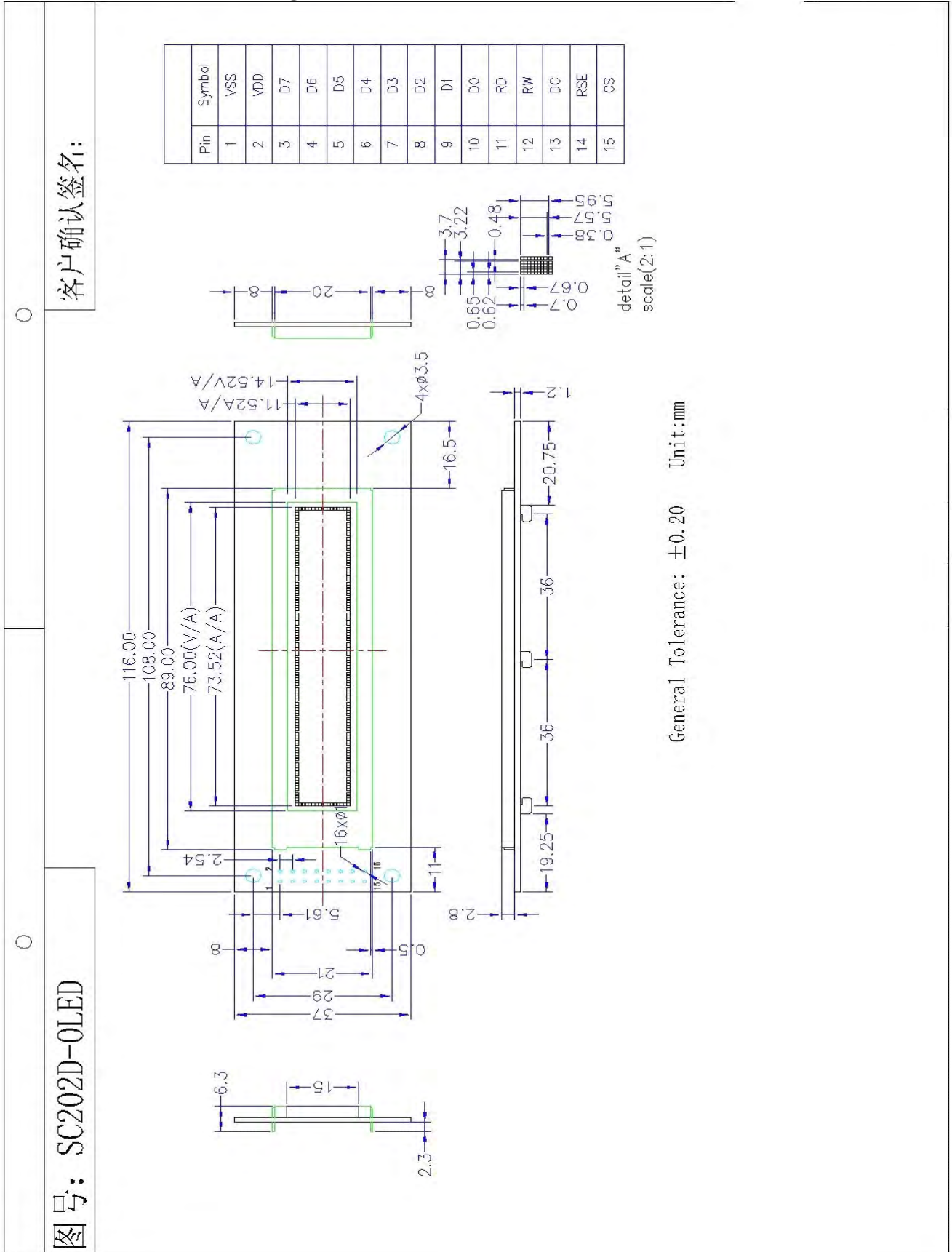
### 1.1 Display Specifications

- 1) Display Mode: Passive Matrix OLED
- 2) Display Color: Yellow(monochrome)
- 3) Drive Duty: 1/16 Duty
- 4) Controller Driver:US2066

### 1.2 Module Features

<b>Items</b>	<b>Specification</b>	<b>Unit</b>
Diagonal A/A Size	2.93	Inch
Number of dots	20 Characters ( 5×8 dots )×2 Lines	dot
Module size	116×37×4	mm
Active Area	73.52×11.52	mm
viewing Area	76×14.52	mm
Character Pitch	3.55×5.95	mm
Character Size	2.97×5.57	mm
Dot Pitch	0.60×0.70	mm
Dot Size	0.57×0.67	mm
General Tolerance	±0.20	mm

## 2.Mechanical Drawing



### 3.Pin Definition

#### 3.1 JP1:

Pin number	Symbol	Type	Function
<b>1</b>	<b>VSS</b>	<b>P</b>	Power supply ground
<b>2</b>	<b>VDD</b>	<b>P</b>	3.3V power supply
<b>3~10</b>	<b>D7~D0</b>	<b>I/O</b>	These are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. When I2C mode is selected, D2 & D1 should be tied together and serve as SDAout & SDAin in application and D0 is the serial clock input SCL.
<b>11</b>	<b>RD</b>	<b>I</b>	When interface to a 6800-series microprocessor, this pin will be used as the Enable(E) signal, When interface to an 8080-microprocessor, this pin receives the Read(RD#)signal.
<b>12</b>	<b>RW</b>	<b>I</b>	This is read/write control input pin connecting to the MCU interface. When interface to a 6800-series microprocessor, Read mode will be carried out when this pin is pulled HIGH and write mode when low. When interface to an 8080-microprocessor, this pin will be the data Write input. When serial interface is selected, this pin must be connected to Vss
<b>13</b>	<b>DC</b>	<b>I</b>	This is DATA/COMMAND control pin. When it is pulled HIGH, the data at D[0~7] is treated as data. When it is pulled LOW, the data at D[0~7] will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.
<b>14</b>	<b>RSE</b>	<b>I</b>	This pin is reset signal input (active LOW)
<b>15</b>	<b>CS</b>	<b>I</b>	This pin is chip select input (active LOW)

#### 3.2 Jump

BS0 /BS1 /BS2:MUC bus interface selection pin.

BS2	BS1	BS0	Interface
0	0	0	Serial Interface
0	0	1	Invalid
0	1	0	I <sup>2</sup> C
0	1	1	Invalid
1	0	0	8-bit 6800 parallel
1	0	1	4-bit 6800 parallel
1	1	0	8-bit 8080 parallel
1	1	1	4-bit 8080 parallel

Notes: "0"connection GND and "1"connection VDD.

#### **4. Absolute Maximum Ratings.**

<b>Parameter</b>	<b>Symbol</b>	<b>Min</b>	<b>Max</b>	<b>Unit</b>	<b>Notes</b>
Supply Voltage for logic	VDD	-0.3	5.5	V	1,2
Supply Voltage for display	VCC	0	13	V	1,2
Operating Temperature	T <sub>OP</sub>	-40	70	°C	-
Storage Temperature	T <sub>STG</sub>	-40	85	°C	-
Life time (100cd/m <sup>2</sup> )		50000	-	hour	3

**Notes1:**

All the above voltages are on the basis of "V<sub>SS</sub> =0V "

**Notes2:**

When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur , also for normal operations, it is desirable to use this module under the conditions according to Section 3."Optics and Electrical Characteristics "If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

**Notes3:**

VCC = 7.25V, Ta = 25° C, 50% Checkerboard.

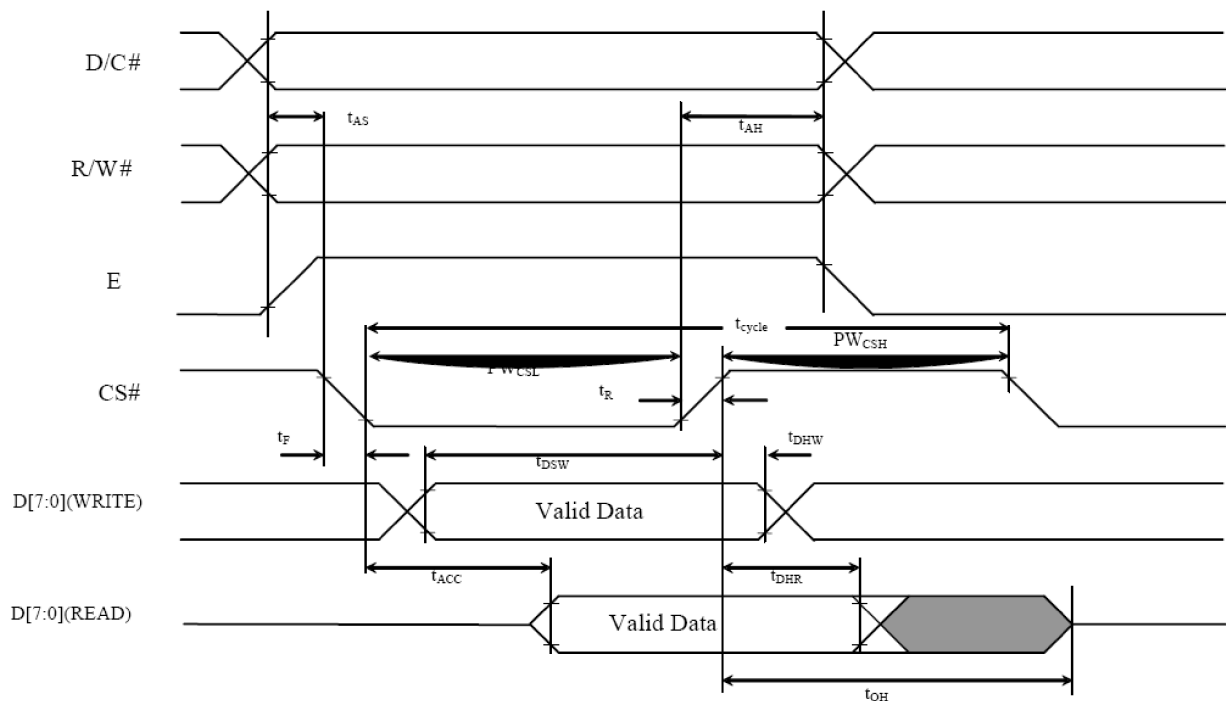
Software configuration follows Section 6.4 Initialization. End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

## 5. Timing Characteristics

### 5.1 68XX-Series MPU Parallel Interface Timing Characteristics:

(TA=25°C, V<sub>DD</sub>-V<sub>SS</sub>=1.65V to 3.3V)

Symbol	parameter	Min	Type	Max	Unit
t <sub>cycle</sub>	Clock Cycle Time (write cycle)	400	-	-	ns
t <sub>AS</sub>	Address Setup time	13	-	-	ns
t <sub>AH</sub>	Address Hold time	17	-	-	ns
t <sub>DSW</sub>	Write Data Setup Time	35	-	-	ns
t <sub>DHW</sub>	Write Data Hold time	18	-	-	ns
t <sub>DHR</sub>	Read Data Hold Time	13	-	-	ns
t <sub>OH</sub>	Output Disable Time	10	-	90	ns
t <sub>ACC</sub>	Access Time (RAM) Access Time (command)	-	-	125	ns
PW <sub>CSL</sub>	Chip Select Low Pulse Width (read RAM)	250	-	-	ns
	Chip Select Low Pulse Width (read command)	250	-	-	ns
	Chip Select Low Pulse Width (write)	50	-	-	ns
PW <sub>CSH</sub>	Chip select High Pulse Width (read)	155	-	-	ns
	Chip Select High Pulse Width (write)	55	-	-	ns
t <sub>R</sub>	Rise Time	-	-	15	ns
t <sub>F</sub>	Fall Time	-	-	15	ns

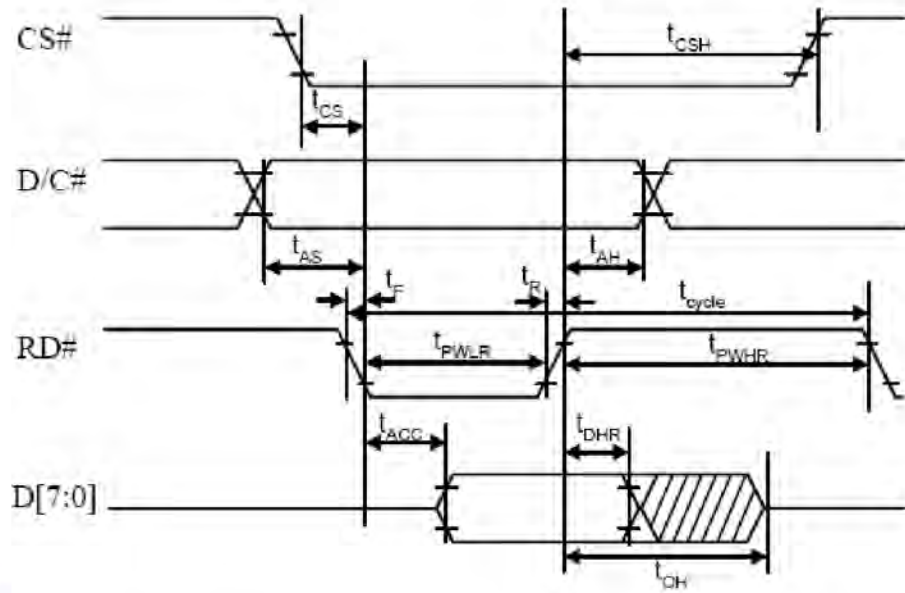


**5.2 80XX-Series MPU Parallel Interface Timing Characteristics:**

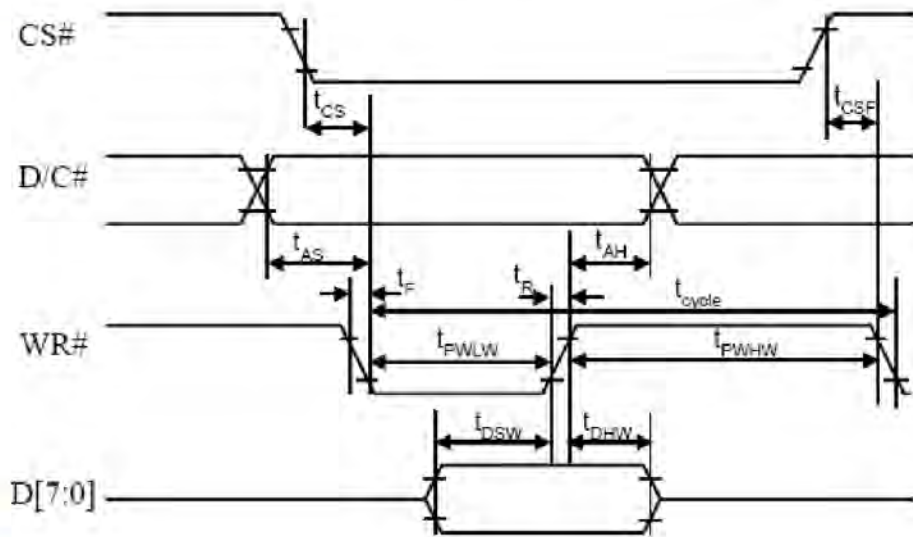
(TA=25°C, V<sub>DD</sub> -V<sub>SS</sub>=1.65V to 3.3V)

Symbol	parameter	Min	Type	Max	Unit
<b>t<sub>cycle</sub></b>	Clock Cycle Time (write cycle)	400	-	-	ns
<b>t<sub>AS</sub></b>	Address Setup time	13	-	-	ns
<b>t<sub>AH</sub></b>	Address Hold time	17	-	-	ns
<b>t<sub>CS</sub></b>	Chip Select time	0	-	-	ns
<b>t<sub>CSH</sub></b>	Chip select Hold Time To read signal	0	-	-	ns
<b>t<sub>CSF</sub></b>	Chip select hold time	0	-	-	ns
<b>t<sub>DSW</sub></b>	Write Data Setup Time	35	-	-	ns
<b>t<sub>DHW</sub></b>	Write Data Hold time	18	-	-	ns
<b>t<sub>DHR</sub></b>	Read Data Hold Time	13	-	-	ns
<b>t<sub>OH</sub></b>	Output Disable Time	10	-	90	ns
<b>t<sub>ACC</sub></b>	Access Time	-	-	125	ns
<b>t<sub>PWLR</sub></b>	Read Low time	250	-	-	ns
<b>t<sub>PWLW</sub></b>	Write Low time	50	-	-	ns
<b>t<sub>PWHR</sub></b>	Read High time	155	-	-	ns
<b>t<sub>PWHW</sub></b>	Write High time	55	-	-	ns
<b>t<sub>R</sub></b>	Rise Time	-	-	15	ns
<b>t<sub>F</sub></b>	Fall Time	-	-	15	ns



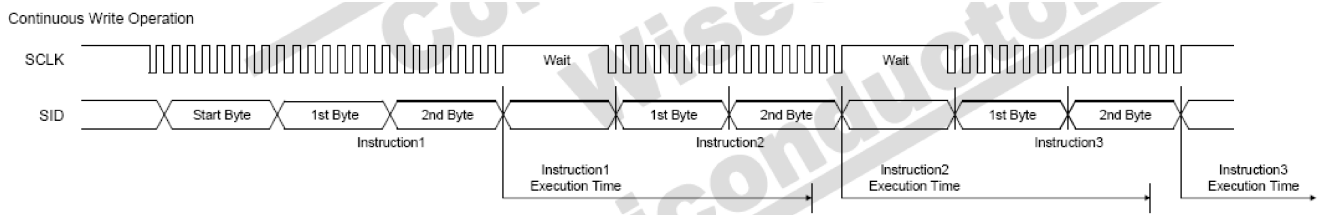
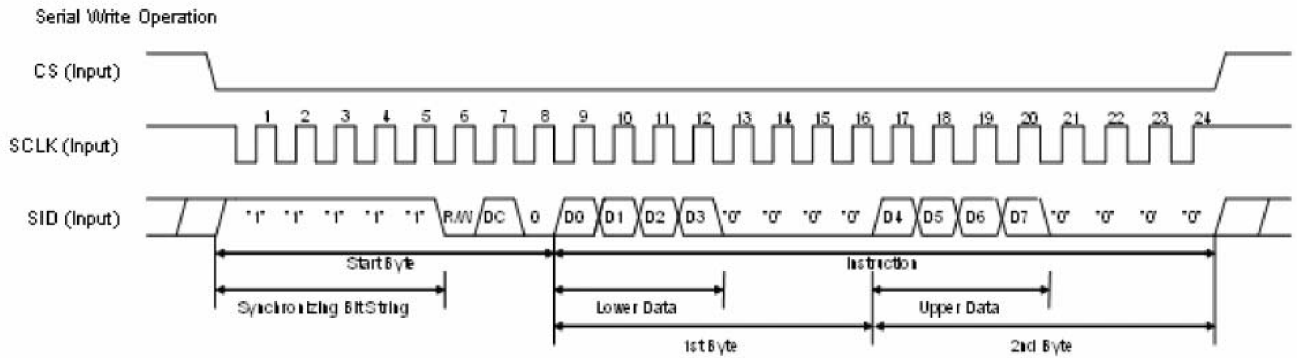


**( Read Timing )**



**( Write Timing )**

### 5.3 Serial Interface Timing Characteristics:



## **6.Reference Sequence**

### **6.1 Commands**

Refer to the Technical Manual for the US2066

### **6.2 Power down and Power up Sequence**

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

#### **6.2.1 Power up Sequence:**

1. Power up VDD
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up VCC
6. Delay 100ms (When VCC is stable)
7. Send Display on command

#### **6.2.2 Power down Sequence:**

1. Send Display off command
2. Power down VCC
3. Delay 100ms (When VCC is reach 0 and panel is completely discharges)
4. Power down VDD

#### **Note :**

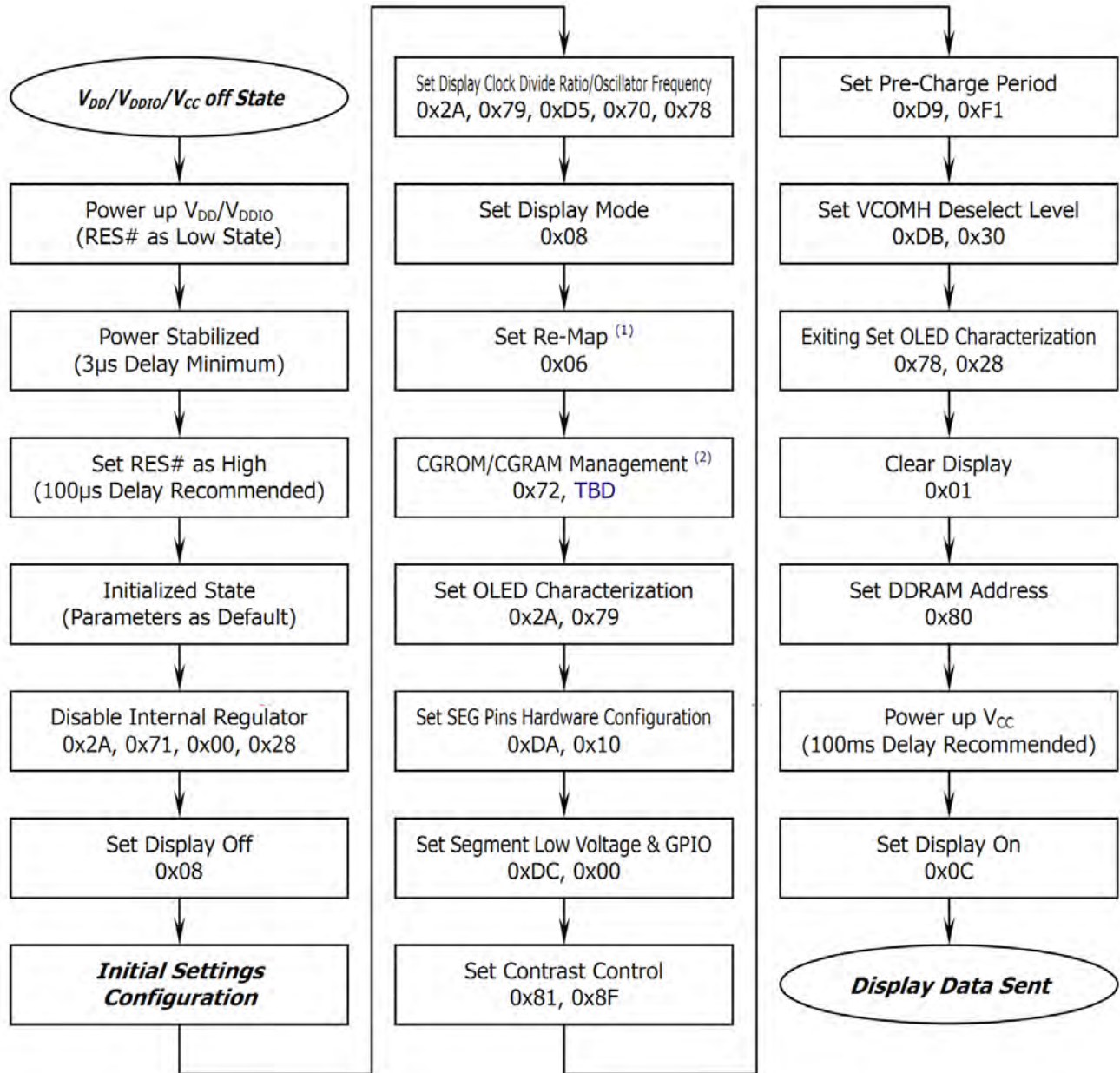
- 1) Since an ESD protection circuit is connected between VDD and VCC inside the driver IC, VCC becomes lower than VDD whenever VDD is ON and VCC is OFF.
- 2) VCC should be kept float (disable) when it is OFF.
- 3) Power Pins (VDD, VCC) can never be pulled to ground under any circumstance.
- 4) VDD should not be power down before VCC power down.

### **6.3 Reset Circuit**

When RES# input is low, the chip is initialized with the following status:

1. Display off, Cursor off, Blink off.
2. Power Down off.
3. 5-dot font is default.
4. Display Shift Disable.
5. CGRAM address is 00h. SEGRAM address is 00h.
6. DDRAM address is 00h.
7. Display start line is set at display RAM address 0
8. Column address counter is set at 0
9. Normal scan direction of the COM outputs
10. Contrast control register is set at 7Fh

### 6.4: 3.3V I/O Application <Power up Sequence>

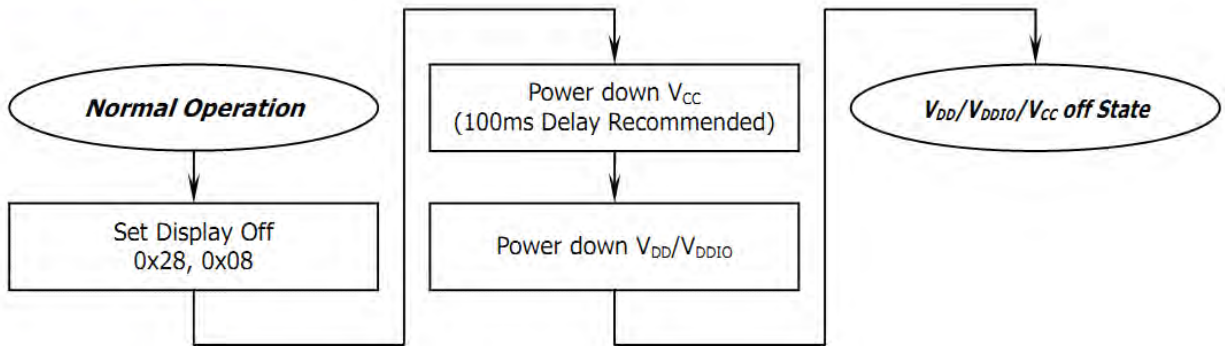


(1) This command could be programmable or defined by pin configuration.

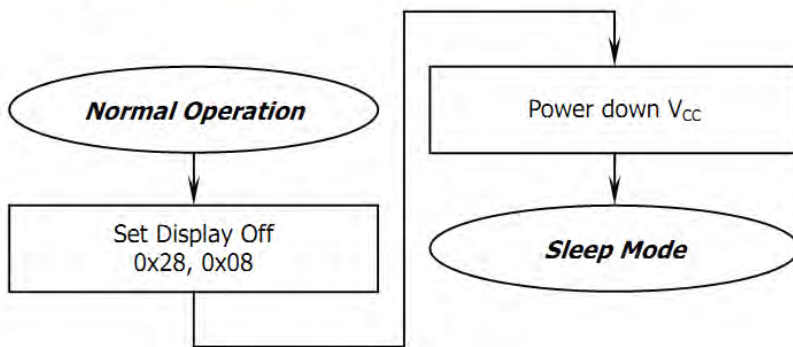
(2) This command could be programmable or defined by pin configuration. The written value of the parameter should depend on the selection from Section Built-in CGROM (Character Generator ROM) and Self-Defined CGRAM (Character Generator RAM)

If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

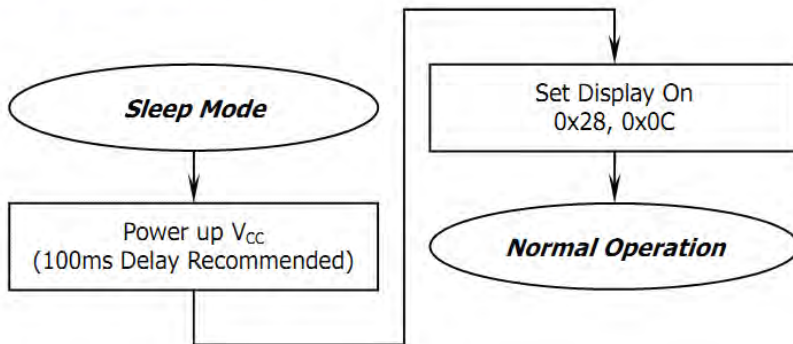
<Power down Sequence>



<Entering Sleep Mode>



<Exiting Sleep Mode>



## 6.5 US2066 CGROM Character Code

### 5.5.1 ROMA

b7-4 \ b3-0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000																
0001	▲	◆	◇	◇	◇	◇	◇	◇	◇	◇	◇	◇	◇	◇	◇	■
0010	!	"	#	\$	%	&	'	(	)	*	+	,	-	.	/	
0011	0	1	2	3	4	5	6	7	8	9	*	+	<	=	>	?
0100	I	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
0101	P	Q	R	S	T	U	V	W	X	Y	Z	A	B	C	D	E
0110	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	
0111	p	q	r	s	t	u	v	w	x	y	z	A	B	C	D	E
1000	0	1	2	3	4	5	6	7	8	9	*	+	<	=	>	?
1001	▲	◆	◇	◇	◇	◇	◇	◇	◇	◇	◇	◇	◇	◇	◇	■
1010	0	1	2	3	4	5	6	7	8	9	*	+	<	=	>	?
1011	0	1	2	3	4	5	6	7	8	9	*	+	<	=	>	?
1100	0	1	2	3	4	5	6	7	8	9	*	+	<	=	>	?
1101	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■
1110	0	1	2	3	4	5	6	7	8	9	*	+	<	=	>	?
1111	0	1	2	3	4	5	6	7	8	9	*	+	<	=	>	?

**6.5.2 RMOB**

b7-4 \ b3-0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000																
0001																
0010																
0011																
0100																
0101																
0110																
0111																
1000																
1001																
1010																
1011																
1100																
1101																
1110																
1111																

**6.5.3 ROMC**

b7-4 \ b3-0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0001	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V
0010	W	X	Y	Z	[	\	^	_	`	{		~				
0011	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0100	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V
0101	W	X	Y	Z	[	\	^	_	`	{		~				
0110	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p
0111	q	r	s	t	u	v	w	x	y	z	{		~			
1000	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1001	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V
1010	W	X	Y	Z	[	\	^	_	`	{		~				
1011																
1100	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1101	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V
1110	W	X	Y	Z	[	\	^	_	`	{		~				
1111																



## 7. QUALITY CONTROL

### 7.1 EastRising Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

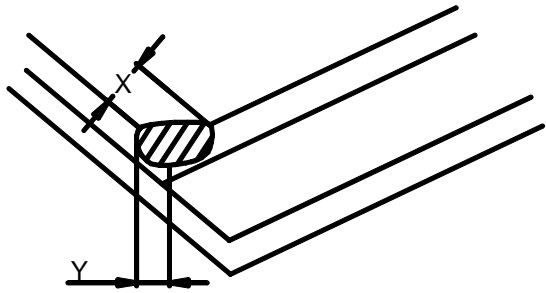
Temperature:	23±5°C
Humidity:	55±15% RH
Fluorescent Lamp:	30W
Distance between the Panel & Lamp:	≥50cm
Distance between the Panel & Eyes of the Inspector:	≥30cm

Finger glove (or finger cover) must be worn by the inspector.  
Inspection table of jig must be anti-electrostatic.

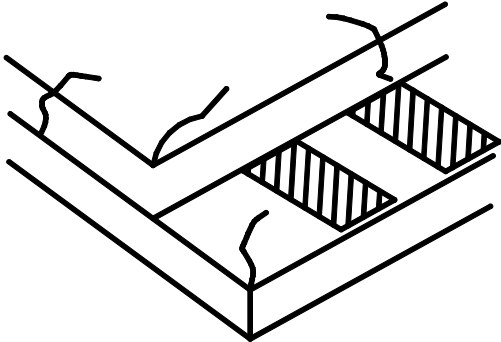

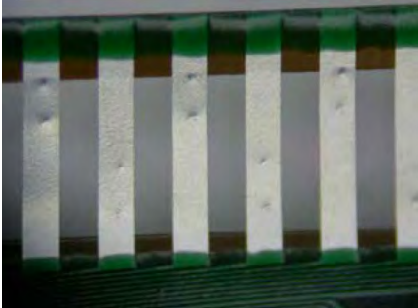
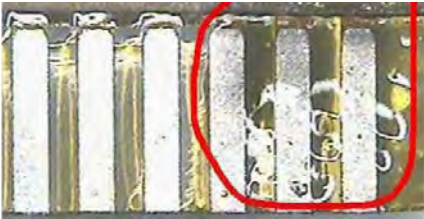
### 7.2 EastRising OLED Display Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

#### 7.2.1 EastRising Cosmetic Check (Display Off) in Non-Active Area

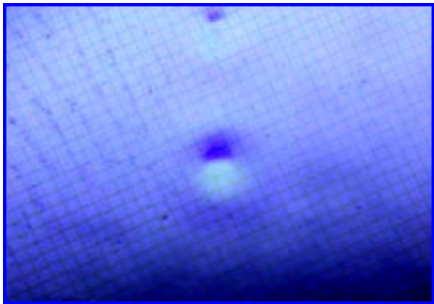
Check Item	Classification	Criteria
Panel General Chipping	Minor	<p>X&gt;6mm (Along with Edge) Y&gt;1mm (Perpendicular to edge)</p> 

7.2.2 EastRising Cosmetic Check (Display Off)in Non-Active Area (Continued)

Check Item	Classification	Criteria
Panel Crack	Minor	<p>Any crack is not allowable</p>  <p>The diagram shows a 3D perspective of a rectangular panel with a crack running across its top surface. The crack is shown as a jagged line. Below the panel, there are two rectangular blocks with diagonal hatching, representing internal components or layers. Arrows point from the text 'Any crack is not allowable' to the crack in the diagram.</p>
Copper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	 <p>The image shows a close-up of a yellow substrate with a circular hole. A small, irregular white mark is visible on the yellow surface near the hole, representing film or trace damage.</p>
Termial Lead Prober Mark	Acceptable	 <p>The image shows a series of vertical metal leads on a green substrate. There are small, dark marks on the leads, which are identified as terminal lead prober marks.</p>
Glue or Contamination on Pin	Minor	 <p>The image shows a series of vertical metal pins on a substrate. A red circle highlights a specific pin that has a white, irregular substance (glue or contamination) on its surface.</p>
Ink marking on Back Side of Panel (Exclude on Film)	Acceptable	Ignore for Any

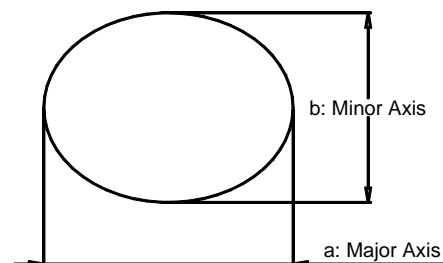
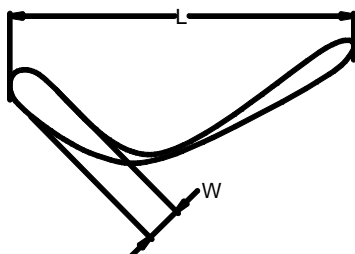
7.2.3 EastRising Cosmetic Check (Display Off) in Active Area

EastRising recommends to execute in clear environment (class 10k) if actual in necessary.


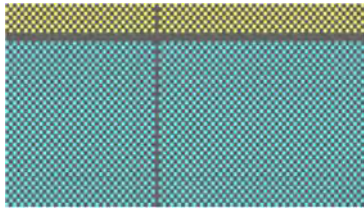
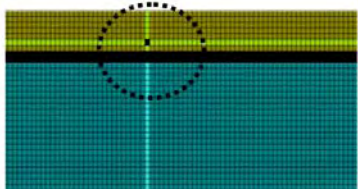
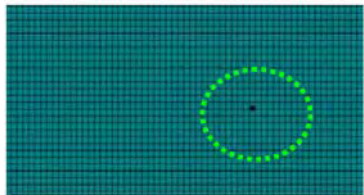
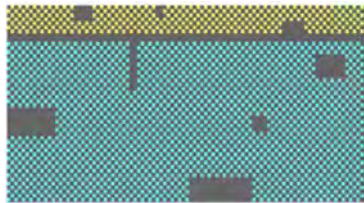
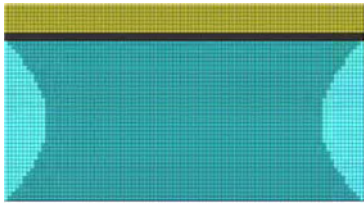
Check Item	Classification	Criteria
Any Dirt & Scratch on Polarizer's Protective Film	Acceptable	Ignore for not Affect the Polarizer
Scratches,Fiber,Line-Shape Defect (On Polarizer)	Minor	$W \leq 0.1$ Ignore $W > 0.1$ $L \leq 2$ $n \leq 1$ $L > 2$ $n = 0$
Dirt, Black Spot, Foreign Material (On Polarizer)	Minor	$\Phi \leq 0.1$ Ignore $0.1 < \Phi \leq 0.25$ $n \leq 1$ $0.25 < \Phi$ $n = 0$
Dent,Bubbles,White Spot (Any Transparent Spot on Polarizer)	Minor	$\Phi \leq 0.5$ Ignore if no Influence on Display $0.5 < \Phi$ $n = 0$ 
Fingerprint ,Flow Mark (On Polarizer)	Minor	Not Allowable

\* Protective film should not be tear off when cosmetic check.

\* Definition of W & L &  $\Phi$ (Unit:mm):  $\Phi = (a+b)/2$



7.2.4 EastRising Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major	

## **7.PRECAUTIONS for USING**

### 8.1 Handling Precautions

- 1) Since the EastRising OLED display panel is being made of glass, do not apply mechanical impacts such as dropping from a high position.
- 2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
- 3) If pressure is applied to the display surface or its neighborhood of the EastRising OLED display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
- 4) The polarizer covering the surface of the OLED display module is soft and easily scratched. Please be careful when handling the OLED display module.
- 5) When the surface of the polarizer of the OLED display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
  - \* Scotch Mending Tape No. 810 or an equivalentNever try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy. Also, pay attention that the following liquid and solvent may spoil the polarizer:
  - \* Water
  - \* Ketone
  - \* Aromatic Solvents
- 6) Hold EastRising OLED display module very carefully when placing OLED display module into the system housing. Do not apply excessive stress or pressure to OLED display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.
- 7) Do not apply stress to the driver IC and the surrounding molded sections.
- 8) Do not disassemble nor modify the OLED display module.
- 9) Do not apply input signals while the logic power is off.
- 10) Pay sufficient attention to the working environments when handling EastRising OLED display modules to prevent occurrence of element breakage accidents by static electricity.
  - \* Be sure to make human body grounding when handling OLED display modules.
  - \* Be sure to ground tools to use or assembly such as soldering irons.
  - \* To suppress generation of static electricity, avoid carrying out assembly work under dry environments.

\* Protective film is being applied to the surface of the display panel of the OLED display module. Be careful since static electricity may be generated when exfoliating the protective film.

11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the EastRising OLED display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).

12) If electric current is applied when the OLED display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

### 8.2 Storage Precautions

- 1) When storing EastRising OLED display modules, put them in static electricity preventive bags avoiding exposure neither to direct sun light nor to lights of fluorescent lamps. and, also, avoiding high temperature and high humidity environment or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from EastRising.) At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.
- 2) If electric current is applied when water drops are adhering to the surface of the OLED display module, when the OLED display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

### 8.3 Designing Precautions

- 1) The absolute maximum ratings are the ratings which cannot be exceeded for OLED display module, and if these values are exceeded, panel damage may be happen.
- 2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.
- 3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)
- 4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
- 5) As for EMI, take necessary measures on the equipment side basically.
- 6) When fastening the OLED display module, fasten the external plastic housing section.

7) If power supply to the EastRising OLED display module is forcibly shut down by such errors as taking out the main battery while the OLED display panel is in operation, we cannot guarantee the quality of this OLED display module.

#### 8.4 Precautions when disposing of the EastRising OLED display modules

1) Request the qualified companies to handle industrial wastes when disposing of the OLED display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

#### 8.5 Other Precautions

1) When an OLED display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur. Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.

2) To protect OLED display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OLED display modules.

- \* Pins and electrodes

- \* Pattern layouts such as the FPC

3) With this OLED display module, the OLED driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OLED driver is exposed to light, malfunctioning may occur.

- \* Design the product and installation method so that the OLED driver may be shielded from light in actual usage.

- \* Design the product and installation method so that the OLED driver may be shielded from light during the inspection processes.

4) Although this OLED display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.

5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.

**That's the end of the datasheet.**