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Revisions

Rev	Description	Date	Approved
X1	Initial Draft	04/10/12	M. NORMAN
A	Release to production	05/03/12	M. NORMAN
B	Changes made to KL25Z XTAL Circuit	05/09/12	M. NORMAN
C	Fixed J10 orientation.	05/21/12	M. NORMAN
CX1	Initial Re-spin Prototype revision	06/29/12	M. NORMAN
D	Re-spin release	07/10/12	M. NORMAN

FREEDOM KL25Z

freescale

Automotive, Industrial & Multi-Market Solutions Group
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ICAP Classification: FCP: FIUO: PUBI: X

Designer: RAFAEL DEL REY	Drawing Title: FRDM-KL25Z		
Drawn by: RAFAEL DEL REY	Page Title: TITLE PAGE		
Approved: MICHAEL NORMAN	Size C	Document Number SCH-27556 | PDF: SPF-27556	Rev D
	Date: Friday, July 13, 2012	Sheet 1 of 5	

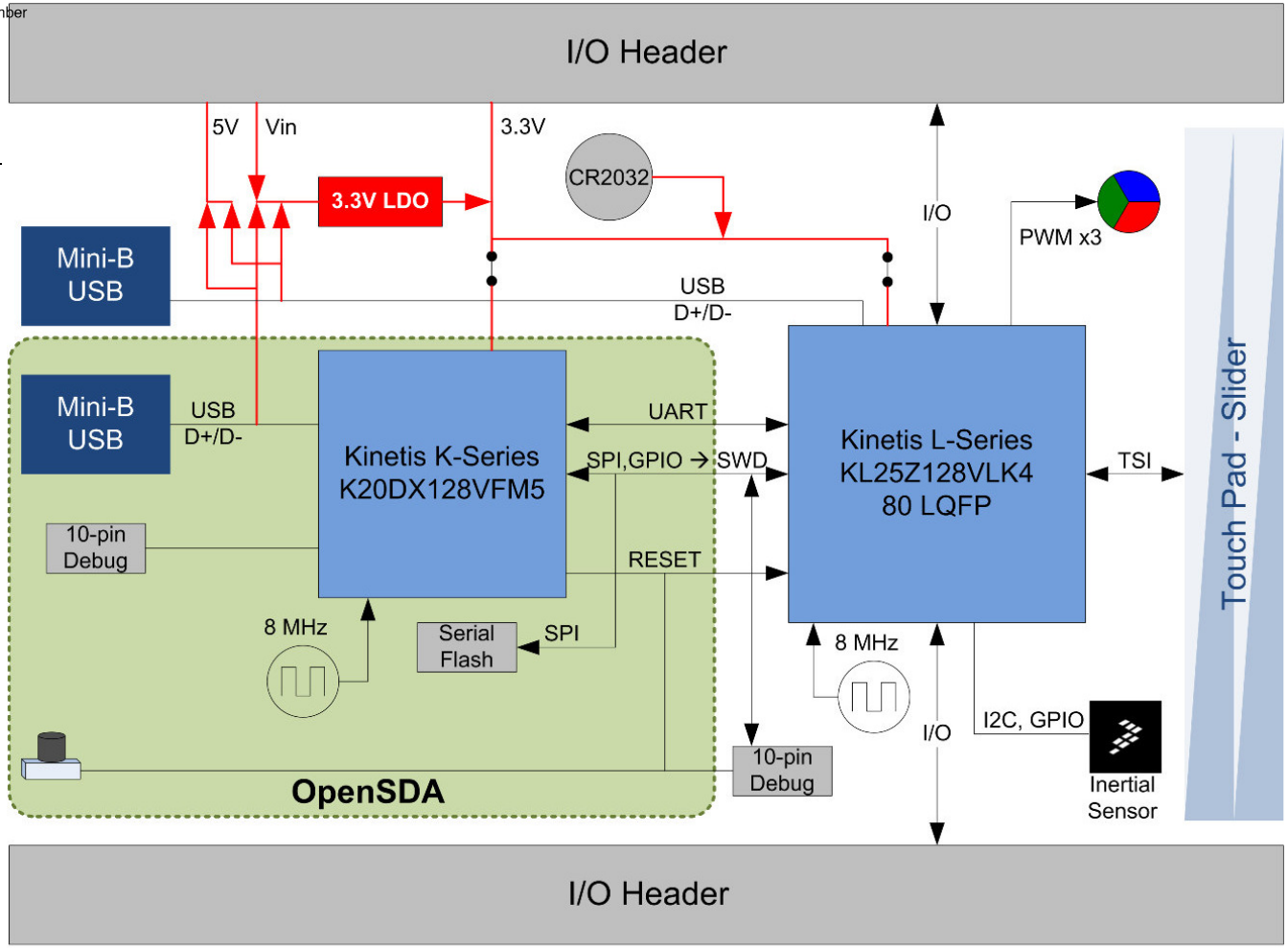
1. Unless Otherwise Specified:
   All resistors are in ohms, 5%, 1/8 Watt
   All capacitors are in uF, 20%, 50V
   All voltages are DC
   All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.



— Indicates optional items that will **not** be populated by default

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Drawing Title: FRDM-KL25Z			
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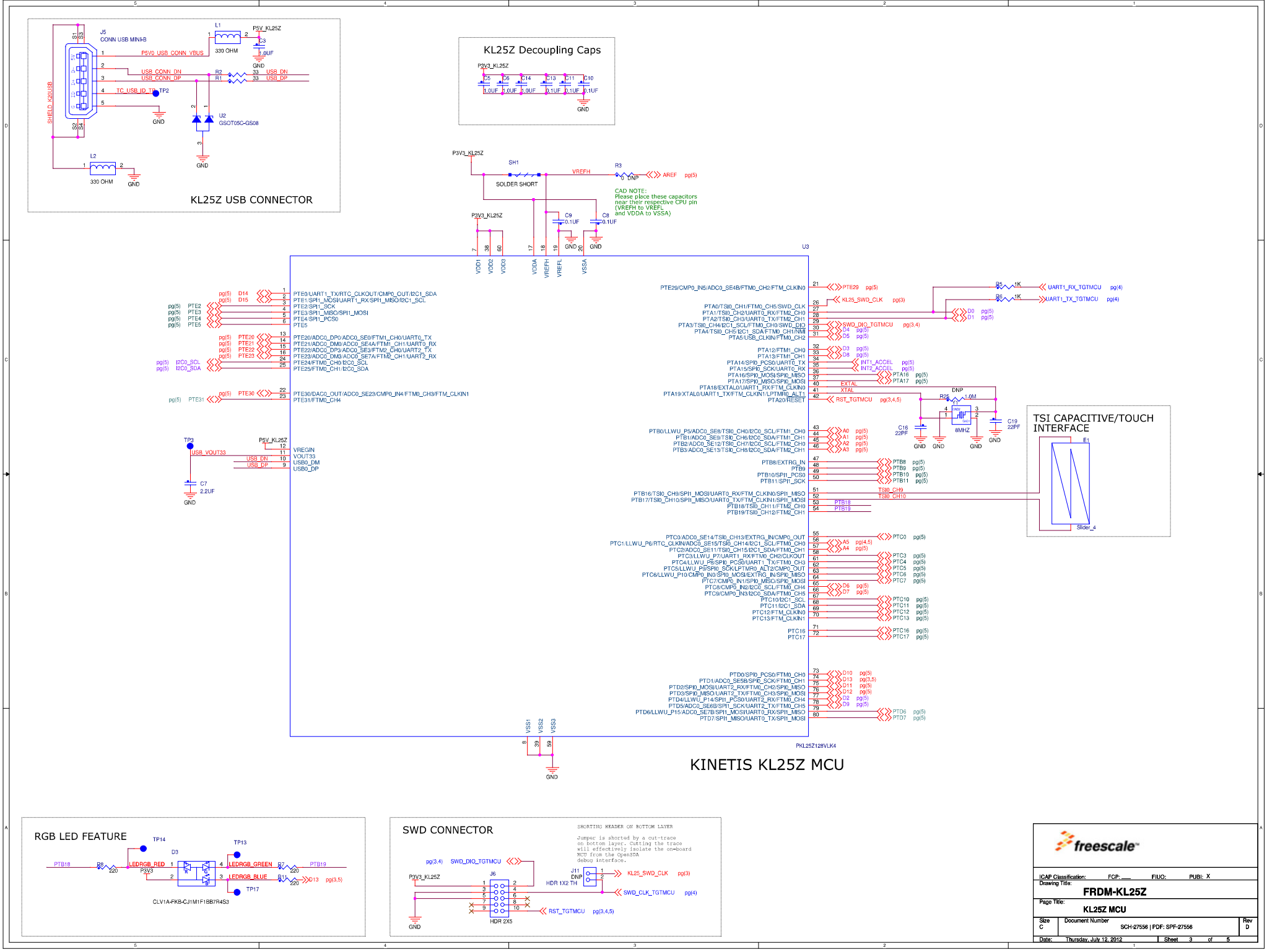
KL25Z USB CONNECTOR
J5
CONN USB MINI-B
SHIELD_K20USB
L1
330 OHM
P5V_KL25Z
C3
1.0UF
P5V0_USB_CONN_VBUS
USB_CONN_DN
USB_CONN_DP
R2
R1
33
USB_DN
USB_DP
TC_USB_ID_TP
TP2
U2
GSOT05C-GS08
L2
330 OHM
GND
KL25Z Decoupling Caps
P3V3_KL25Z
C5
C6
C14
C13
C11
C10
1.0UF
0.1UF
SH1
SOLDER SHORT
VREFH
R3
0 DNP
AREF
pg(5)
CAD NOTE:
Please place these capacitors
near their respective CPU pin
(VREFH to VREFL
and VDDA to VSSA)
C9
0.1UF
C8
0.1UF
U3
VDD1
VDD2
VDD3
VDDA
VREFH
VREFL
VSSA
PTE0/UART1_TX/RTC_CLKOUT/CMP0_OUT/I2C1_SDA
PTE1/SPI1_MOSI/UART1_RX/SPI1_MISO/I2C1_SCL
PTE2/SPI1_SCK
PTE3/SPI1_MISO/SPI1_MOSI
PTE4/SPI1_PCS0
PTE5
PTE20/ADC0_DP0/ADC0_SE0/FTM1_CH0/UART0_TX
PTE21/ADC0_DM0/ADC0_SE4A/FTM1_CH1/UART0_RX
PTE22/ADC0_DP3/ADC0_SE3/FTM2_CH0/UART2_TX
PTE23/ADC0_DM3/ADC0_SE7A/FTM2_CH1/UART2_RX
PTE24/FTM0_CH0/I2C0_SCL
PTE25/FTM0_CH1/I2C0_SDA
PTE30/DAC0_OUT/ADC0_SE23/CMP0_IN4/FTM0_CH3/FTM_CLKIN1
PTE31/FTM0_CH4
PTE29/CMP0_IN5/ADC0_SE4B/FTM0_CH2/FTM_CLKIN0
PTA0/TSI0_CH1/FTM0_CH5/SWD_CLK
PTA1/TSI0_CH2/UART0_RX/FTM2_CH0
PTA2/TSI0_CH3/UART0_TX/FTM2_CH1
PTA3/TSI0_CH4/I2C1_SCL/FTM0_CH0/SWD_DIO
PTA4/TSI0_CH5/I2C1_SDA/FTM0_CH1/NMI
PTA5/USB_CLKIN/FTM0_CH2
PTA12/FTM1_CH0
PTA13/FTM1_CH1
PTA14/SPI0_PCS0/UART0_TX
PTA15/SPI0_SCK/UART0_RX
PTA16/SPI0_MOSI/SPI0_MISO
PTA17/SPI0_MISO/SPI0_MOSI
PTA18/EXTAL0/UART1_RX/FTM_CLKIN0
PTA19/XTAL0/UART1_TX/FTM_CLKIN1/LPTMR0_ALT1
PTA20/RESET
PTB0/LLWU_P5/ADC0_SE8/TSI0_CH0/I2C0_SCL/FTM1_CH0
PTB1/ADC0_SE9/TSI0_CH6/I2C0_SDA/FTM1_CH1
PTB2/ADC0_SE12/TSI0_CH7/I2C0_SCL/FTM2_CH0
PTB3/ADC0_SE13/TSI0_CH8/I2C0_SDA/FTM2_CH1
PTB8/EXTRG_IN
PTB9
PTB10/SPI1_PCS0
PTB11/SPI1_SCK
PTB16/TSI0_CH9/SPI1_MOSI/UART0_RX/FTM_CLKIN0/SPI1_MISO
PTB17/TSI0_CH10/SPI1_MISO/UART0_TX/FTM_CLKIN1/SPI1_MOSI
PTB18/TSI0_CH11/FTM2_CH0
PTB19/TSI0_CH12/FTM2_CH1
PTC0/ADC0_SE14/TSI0_CH13/EXTRG_IN/CMP0_OUT
PTC1/LLWU_P6/RTC_CLKIN/ADC0_SE15/TSI0_CH14/I2C1_SCL/FTM0_CH0
PTC2/ADC0_SE11/TSI0_CH15/I2C1_SDA/FTM0_CH1
PTC3/LLWU_P7/UART1_RX/FTM0_CH2/CLKOUT
PTC4/LLWU_P8/SPI0_PCS0/UART1_TX/FTM0_CH3
PTC5/LLWU_P9/SPI0_SCK/LPTMR0_ALT2/CMP0_OUT
PTC6/LLWU_P10/CMP0_IN0/SPI0_MOSI/EXTRG_IN/SPI0_MISO
PTC7/CMP0_IN1/SPI0_MISO/SPI0_MOSI
PTC8/CMP0_IN2/I2C0_SCL/FTM0_CH4
PTC9/CMP0_IN3/I2C0_SDA/FTM0_CH5
PTC10/I2C1_SCL
PTC11/I2C1_SDA
PTC12/FTM_CLKIN0
PTC13/FTM_CLKIN1
PTC16
PTC17
PTD0/SPI0_PCS0/FTM0_CH0
PTD1/ADC0_SE5B/SPI0_SCK/FTM0_CH1
PTD2/SPI0_MOSI/UART2_RX/FTM0_CH2/SPI0_MISO
PTD3/SPI0_MISO/UART2_TX/FTM0_CH3/SPI0_MOSI
PTD4/LLWU_P14/SPI1_PCS0/UART2_RX/FTM0_CH4
PTD5/ADC0_SE6B/SPI1_SCK/UART2_TX/FTM0_CH5
PTD6/LLWU_P15/ADC0_SE7B/SPI1_MOSI/UART0_RX/SPI1_MISO
PTD7/SPI1_MISO/UART0_TX/SPI1_MOSI
VREGIN
VOUT33
USB0_DM
USB0_DP
USB_VOUT33
C7
2.2UF
VSS1
VSS2
VSS3
PKL25Z128VLK4
KINETIS KL25Z MCU
UART1_RX_TGTMCU
UART1_TX_TGTMCU
SWD_DIO_TGTMCU
KL25_SWD_CLK
INT1_ACCEL
INT2_ACCEL
EXTAL
XTAL
RST_TGTMCU
R25
1.0M
8MHZ
C16
22PF
C19
22PF
DNP
TSI CAPACITIVE/TOUCH
INTERFACE
E1
Slider_4
RGB LED FEATURE
TP14
TP13
TP17
D3
PTB18
R8
220
LEDRGB_RED
LEDRGB_GREEN
LEDRGB_BLUE
R7
220
R11
220
PTB19
D13
pg(3,5)
CLV1A-FKB-CJ1M1F1BB7R4S3
SWD CONNECTOR
SHORTING HEADER ON BOTTOM LAYER
Jumper is shorted by a cut-trace
on bottom layer. Cutting the trace
will effectively isolate the on-board
MCU from the OpenSDA
debug interface.
J6
HDR 2X5
J11
HDR 1X2 TH
KL25_SWD_CLK
SWD_CLK_TGTMCU
RST_TGTMCU
freescale
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FCP:
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PUB1: X
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KL25Z MCU
Size
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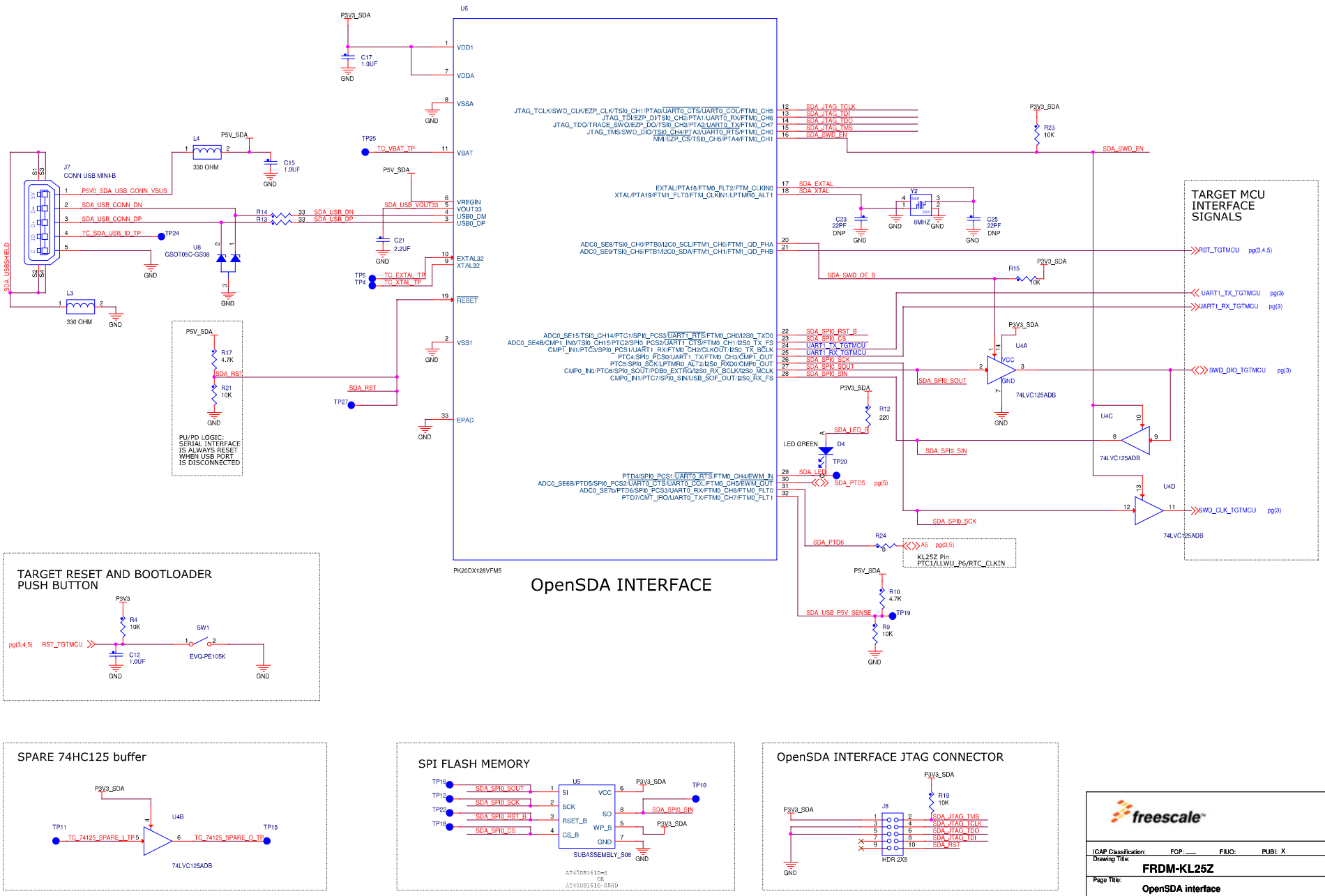
OpenSDA INTERFACE
U6
PK20DX128VFM5
VDD1
VDDA
VSSA
VBAT
VREGIN
VOUT33
USB0_DM
USB0_DP
EXTAL32
XTAL32
RESET
VSS1
EPAD
JTAG_TCLK/SWD_CLK/EZP_CLK/TSI0_CH1/PTA0/UART0_CTS/UART0_COL/FTM0_CH5
JTAG_TDI/EZP_DI/TSI0_CH2/PTA1/UART0_RX/FTM0_CH6
JTAG_TDO/TRACE_SWO/EZP_DO/TSI0_CH3/PTA2/UART0_TX/FTM0_CH7
JTAG_TMS/SWD_DIO/TSI0_CH4/PTA3/UART0_RTS/FTM0_CH0
NMI/EZP_CS/TSI0_CH5/PTA4/FTM0_CH1
EXTAL/PTA18/FTM0_FLT2/FTM_CLKIN0
XTAL/PTA19/FTM1_FLT0/FTM_CLKIN1/LPTMR0_ALT1
ADC0_SE8/TSI0_CH0/PTB0/I2C0_SCL/FTM1_CH0/FTM1_QD_PHA
ADC0_SE9/TSI0_CH6/PTB1/I2C0_SDA/FTM1_CH1/FTM1_QD_PHB
ADC0_SE15/TSI0_CH14/PTC1/SPI0_PCS3/UART1_RTS/FTM0_CH0/I2S0_TXD0
ADC0_SE4B/CMP1_IN0/TSI0_CH15/PTC2/SPI0_PCS2/UART1_CTS/FTM0_CH1/I2S0_TX_FS
CMP1_IN1/PTC3/SPI0_PCS1/UART1_RX/FTM0_CH2/CLKOUT/I2S0_TX_BCLK
PTC4/SPI0_PCS0/UART1_TX/FTM0_CH3/CMP1_OUT
PTC5/SPI0_SCK/LPTMR0_ALT2/I2S0_RXD0/CMP0_OUT
CMP0_IN0/PTC6/SPI0_SOUT/PDB0_EXTRG/I2S0_RX_BCLK/I2S0_MCLK
CMP0_IN1/PTC7/SPI0_SIN/USB_SOF_OUT/I2S0_RX_FS
PTD4/SPI0_PCS1/UART0_RTS/FTM0_CH4/EWM_IN
ADC0_SE6B/PTD5/SPI0_PCS2/UART0_CTS/UART0_COL/FTM0_CH5/EWM_OUT
ADC0_SE7b/PTD6/SPI0_PCS3/UART0_RX/FTM0_CH6/FTM0_FLT0
PTD7/CMT_IRO/UART0_TX/FTM0_CH7/FTM0_FLT1
SDA_JTAG_TCLK
SDA_JTAG_TDI
SDA_JTAG_TDO
SDA_JTAG_TMS
SDA_SWD_EN
SDA_EXTAL
SDA_XTAL
SDA_SWD_OE_B
SDA_SPI0_RST_B
SDA_SPI0_CS
UART1_TX_TGTMCU
UART1_RX_TGTMCU
SDA_SPI0_SCK
SDA_SPI0_SOUT
SDA_SPI0_SIN
SDA_LED_H
SDA_LED
SDA_PTD5
SDA_PTD6
SDA_USB_P5V_SENSE
SDA_USB_DN
SDA_USB_DP
SDA_USB_VOUT33
TC_VBAT_TP
TC_EXTAL_TP
TC_XTAL_TP
SDA_RST
P3V3_SDA
P5V_SDA
C17 1.0UF
C15 1.0UF
C21 2.2UF
C23 22PF DNP
C25 22PF DNP
Y2 8MHZ
R23 10K
R15 10K
R12 220
R10 4.7K
R9 10K
R24 0
R14 33
R13 33
R17 4.7K
R21 10K
L4 330 OHM
L3 330 OHM
J7 CONN USB MINI-B
P5V_SDA_USB_CONN_VBUS
SDA_USB_CONN_DN
SDA_USB_CONN_DP
TC_SDA_USB_ID_TP
SDA_USBSHIELD
U8 GSOT05C-GS08
TP24
TP25
TP5
TP4
TP27
TP20
TP19
D4 LED GREEN
U4A 74LVC125ADB
U4C 74LVC125ADB
U4D 74LVC125ADB
SWD_DIO_TGTMCU
SWD_CLK_TGTMCU
RST_TGTMCU
A5
KL25Z Pin PTC1/LLWU_P6/RTC_CLKIN
PU/PD LOGIC: SERIAL INTERFACE IS ALWAYS RESET WHEN USB PORT IS DISCONNECTED
TARGET MCU INTERFACE SIGNALS
TARGET RESET AND BOOTLOADER PUSH BUTTON
P3V3
R4 10K
SW1 EVQ-PE105K
C12 1.0UF
SPARE 74HC125 buffer
U4B
TP11
TP15
TC_74125_SPARE_I_TP
TC_74125_SPARE_O_TP
SPI FLASH MEMORY
U5
SUBASSEMBLY_S08
AT45DB161D-SU
OR
AT45DB161E-SSHD
TP10
OpenSDA INTERFACE JTAG CONNECTOR
J8 HDR 2X5
R19 10K
freescale
ICAP Classification: FCP: ___ FIUO: PUB: X
Drawing Title: FRDM-KL25Z
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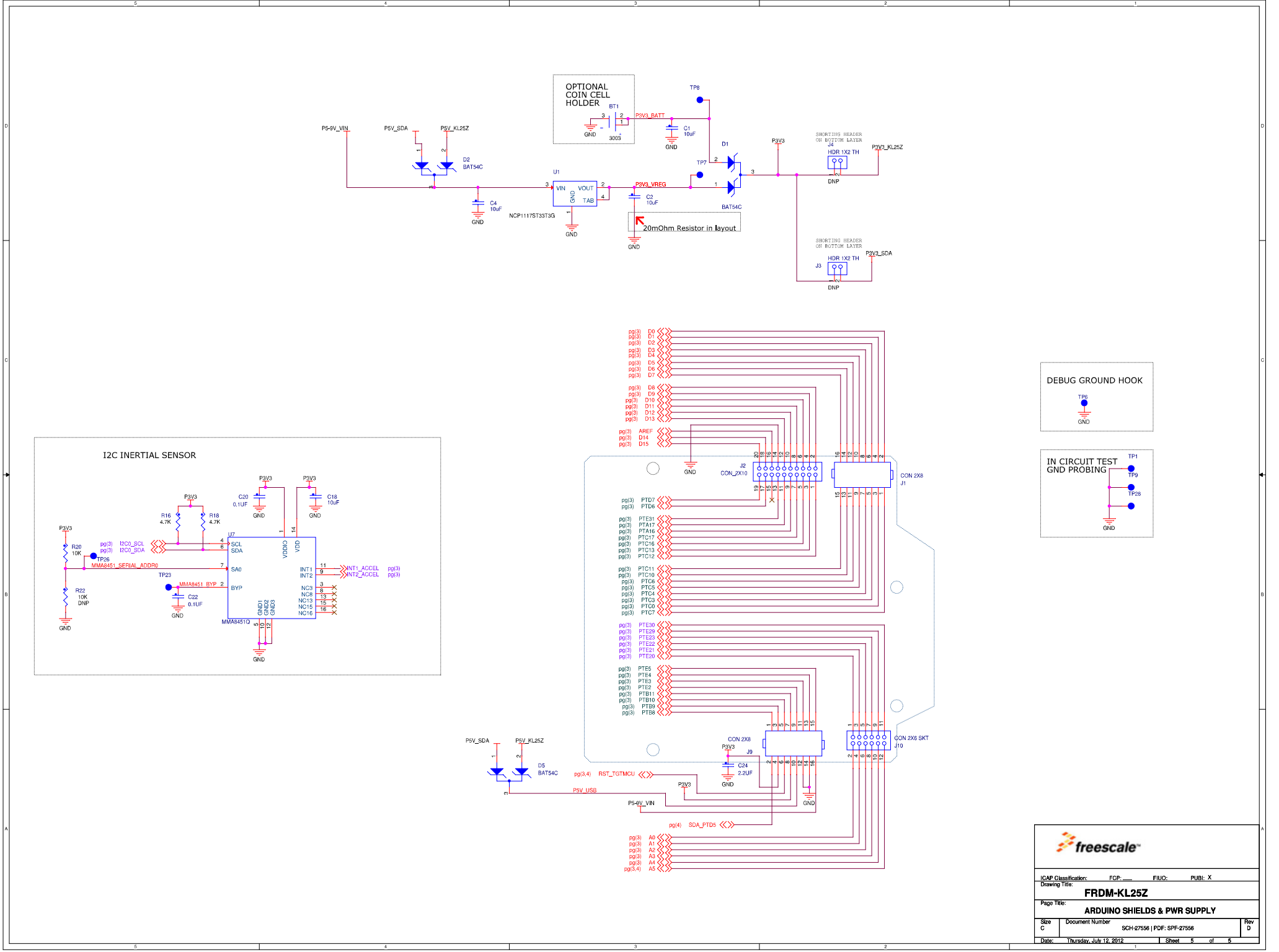

freescale

ICAP Classification:	FCP: ___	FIUO:	PUBI: X
Drawing Title:	FRDM-KL25Z		
Page Title:	ARDUINO SHIELDS & PWR SUPPLY		
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