S1SBP6A

Bio-Processor

Revision 1.00
October 2020

User's Manual

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Chip Handling Guide

Precaution against Electrostatic Discharge

When using semiconductor devices, ensure that the environment is protected against static electricity:

1. Wear antistatic clothes and use earth band.
2. All objects that are in direct contact with devices must be made up of materials that do not produce static electricity.
3. Ensure that the equipment and work table are earthed.
4. Use ionizer to remove electron charge.

Contamination

Do not use semiconductor products in an environment exposed to dust or dirt adhesion.

Temperature/Humidity

Semiconductor devices are sensitive to:

- Environment
- Temperature
- Humidity

High temperature or humidity deteriorates the characteristics of semiconductor devices. Therefore, do not store or use semiconductor devices in such conditions.

Mechanical Shock

Do not to apply excessive mechanical shock or force on semiconductor devices.

Chemical

Do not expose semiconductor devices to chemicals because exposure to chemicals leads to reactions that deteriorate the characteristics of the devices.

Light Protection

In non- Epoxy Molding Compound (EMC) package, do not expose semiconductor IC to bright light. Exposure to bright light causes malfunctioning of the devices. However, a few special products that utilize light or with security functions are exempted from this guide.

Radioactive, Cosmic and X-ray

Radioactive substances, cosmic ray, or X-ray may influence semiconductor devices. These substances or rays may cause a soft error during a device operation. Therefore, ensure to shield the semiconductor devices under environment that may be exposed to radioactive substances, cosmic ray, or X-ray.

EMS (Electromagnetic Susceptibility)

Strong electromagnetic wave or magnetic field may affect the characteristic of semiconductor devices during the operation under insufficient PCB circuit design for Electromagnetic Susceptibility (EMS).

Revision History

Revision No.	Date	Description	Author(s)
1.00	Oct. 12, 2020	• First release	DaeHwan Kim

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List of Conventions

Register RW Access Type Conventions

Type	Definition	Description
R	Read Only	The application has permission to read the Register field. Writes to read-only fields have no effect.
W	Write Only	The application has permission to write in the Register field.
RW	Read & Write	The application has permission to read and writes in the Register field. The application sets this field by writing 1'b1 and clears it by writing 1'b0.

Register Value Conventions

Expression	Description
x	Undefined bit
X	Undefined multiple bits
?	Undefined, but depends on the device or pin status
Device dependent	The value depends on the device
Pin value	The value depends on the pin status

Reset Value Conventions

Expression	Description
0	Clears the register field
1	Sets the register field
x	Don't care condition

Warning: Some bits of control registers are driven by hardware or write operation only. As a result the indicated reset value and the read value after reset might be different.

List of Acronyms

Acronyms	Descriptions
ADC	Analog to Digital Converter
AES	Advanced Encryption Standard
AFE	Analog Front End
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
BIA	Bioelectrical Impedance Analysis
BOR	Brown-Out Reset
CDM	Charged Device Model
CLK	Clock
CMRR	Common Mode Rejection Ratio
DAC	Digital to Analog Converter
DCC	DC Offset Cancellation
DC-DC	DC to DC Voltage Converter
DSP	Digital Signal Processing
DTRNG	Digital True Random Number Generator
DVFS	Dynamic Voltage and Frequency Scaling
ECG	Electrocardiography
ENOB	Effective Number Of Bit
fCLK	Modulator Clock
Fin	Input Frequency
FPU	Floating-Point Unit
FRC	Free-Running Counter
Fs	Sampling Frequency
FS	Full Scale
GPIO	General Purpose I/O
HBM	Human Body Model
HPF	High Pass Filter
I2C	Inter-Integrated Circuits
IA	Instrumentation Amplifier
IDC	Incremental Data Converter
LDO	Low-Dropout Regulator
LPF	Low Pass Filter
MA	Motion Artifact
MCU	Micro Control Unit

Acronyms	Descriptions
µDMAC	Micro Direct Memory Access Controller
MSPS	Mega Sample Per Second
OS	Operating System
OSC	Oscillator
PFM	Pulse Frequency Modulation
PGA	Programmable Gain Amplifier
POR	Power On Reset
PLL	Phase-locked Loop
PPG	Photoplethysmography
PWM	Pulse Width Modulation
RX	Receiver
RTC	Real-Time Clock
RTI	Referred to Input
SAR	Successive Approximation
SFR	Special Function Register
SNH	Sample-and-Hold
SPI	Serial Peripheral Interface
SPS	Sample Per Second
SRC	Sample Rate Converter
SRP	Samsung Reconfigurable Processor
Ta	Ambient Temperature
Tstg	Storage Temperature
THD	Total Harmonic Distortion
TIA	Trans impedance Amplifier
Tj	Junction Temperature
TMPX	Test Multiplexer
TX	Transmitter
UART	Universal Asynchronous Receiver and Transmitter
VCMI	Input Common Mode Voltage
VCO	Voltage Controlled Oscillator
WFE	Wait For Event
WFI	Wait For Interrupt
WLP	Wafer Level Package
XiP	eXecution-in-Place

1 Product Overview

This chapter includes the following sections:

- Introduction
- Key features
- Block diagram

1.1 Introduction

S1SBP6A is a low-power bio-processor targeting multiple bio-sensor data acquisition and processing for healthcare and other applications. S1SBP6A supports a wide range of on-chip bio-sensor readouts such as Electrocardiography (ECG), Bioelectrical Impedance Analysis (BIA), optical (Photoplethysmography, PPG), and Galvanic Skin Response (GSR). In addition, General Purpose (GP) analog/digital interfaces allow acquiring data from external analog or digital sensors in a synchronized manner.

S1SBP6A integrates a Micro Controller Unit (MCU) powered by an ARM Cortex-M4 with Floating Point Unit (FPU) engine to improve the signal quality in real-time. And, Slim Samsung Reconfigurable Processor (SlimSRP) is utilized as a Digital Signal Processor (DSP) to improve the power efficiency of on-chip signal processing. In addition, S1SBP6A embeds 2 MB Flash, 256 KB SRAM for MCU, and 160 KB SRAM for DSP. Cortex-M4 core features the degrees of freedom of on-chip processing capability and DSP offers the efficient ways to implement various applications. Also, standard digital interfaces such as SPI, I2C, UART, and GPIO are supported for external communications.

Following are the features applied in the S1SBP6A:

- Clock gating
- Power gating with fine-grained power domains
- On-chip flash memory (2 MB)
- On-chip SRAM (256 KB for MCU and 160 KB for DSP)
- Dedicated low-power Analog Front Ends (AFEs) for ECG, PPG, BIA, and GSR applications
- Integrated LED drivers for PPG and analog current signal synthesizer for BIA
- Sample Rate Converter (SRC) as a hardware accelerator
- 12b GP analog readouts
- Real Time Clock (RTC) with system control
- Built-in Low-Dropout Regulators (LDOs) along with system POR and BOR
- Embedded PLL and Oscillators (OSC)
- Security IPs such as Digital True Random Number Generator (DTRNG) and Advanced Encryption Standard (AES)
- Versatile digital interfaces

1.2 Features

S1SBP6A supports the following features:

- **Single channel ECG readout with built-in High Pass Filter (HPF)**
  - Low-noise of 3.5 μV_{rms} (0.5 Hz - 250 Hz)
  - High common-mode rejection capability, CMRR > 80 dB
  - High impedance electrode interface
  - Maximum of 10 mV_{p-p} ECG inputs without significant signal distortion
  - Flexible gain and bandwidth control
  - Gain of 100 V/V - 600 V/V, bandwidth of 75 Hz - 250 Hz
  - 12b, 1 kSPS/8 kSPS digital conversion
  - Built-in body bias driver capable of driving up to 10 μA current
  - Built-in HPF (< 0.5 Hz) to be tolerable to more than ±300 mV electrode offset
- **BIA readout with integrated current source**
  - Four points (tetra-polar electrode system) complex impedance measurements
  - 6b, 1 MSPS/4 MSPS sine-wave generation
  - Multi-frequency current excitation ranging from 1 kHz to 1 MHz
  - 12b, 1 kSPS/8 kSPS impedance conversion
  - Impedance calibration with external resistors
- **PPG readout with integrated LED drivers**
  - Built-in flexible LED driver with four independent current sink DACs
    - Maximum of four LEDs with different wavelengths (Green, Red, IR)
    - Flexible LED driving current level
    - 0 - 100 mA with 0.78 mA/step, or 0 - 50 mA with 0.39 mA/step
    - Flexible LED current pulse repetition
    - 100 Hz - 1 kHz LED pulse repetition rate with minimum 50 μs LED on time
  - Two synchronous Photo Diode (PD) readouts with ambient light sampling
    - Built-in DC level restoration with ±16 μA (6b) photocurrent cancellation
    - Wide dynamic range readout (10 kΩ - 2 MΩ) Low-noise (integrated over 0.5 Hz - 20 Hz)
    - Ambient light sampling synchronous to LED pulse
    - Maximum of four pulse slots synchronous signal sampling for each readout front end
    - 24b, 1 kSPS**/**pulse digitization
- **GSR readouts with integrated voltage sources**
  - Two points (bipolar electrode system) conductance measurements
  - Built-in DC voltage source with DC/AC-mode (4 Hz, Typ.) outputs
  - Wide dynamic range conductance measurement (0.05 μS - 100 μS)
  - 24b, 500 SPS conductance conversion

- **GP analog interfaces**
  - 12b, 1 kSPS/8 kSPS GP analog readouts
    - Voltage Gain Amplifier (VGA), Trans-Impedance Amplifier (TIA), Low Pass Filter (LPF) input interfaces
    - Wide range of parameter programmability
    - Synchronous data acquisition to the other AFEs
    - Digital data decimation
- **Analog peripherals**
  - Four integrated LDOs (1.1 V) to supply AFE, DSP/MCU, memory, and clock domain
  - Built-in Power On Reset (POR), and Brown-Out Reset (BOR)
  - Built-in PLL (102.4 MHz) and oscillators (4.096 MHz, 24.576 MHz)
  - Built-in bandgap reference and junction temperature sensor
- **Micro controller unit**
  - ARM Cortex-M4 with FPU with maximum 102.4 MHz operation
  - 2 MB embedded Flash and 256 KB SRAM
  - SlimSRP with 160 KB SRAM which is shared by MCU
  - Sample Rate Converter (SRC) as a hardware accelerator
  - 32 channel Micro Direct Memory Access Controller (µDMAC)
  - Seven Timers, one Pulse Width Modulation (PWM) Timer, one Dual-Input Timer, one Watchdog, and one Real-Time Clock (RTC)
  - Serial Flash Interface with eXecution-in-Place (XiP) capability
  - JTAG/software interface for debug
  - Clock Management Unit (CMU) and Power Management Unit (PMU)
  - Digital True Random Number Generator (DTRNG) and Advanced Encryption Standard (AES)
- **Digital interfaces**
  - Five Inter-Integrated Circuits (I2C)
  - Five Serial Peripheral Interfaces (SPI)
  - Three Universal Asynchronous Receiver and Transmitters (UART)
  - 48 General Purpose I/Os (GPIO)
- **Package**
  - 154 pin WLP 4.76 × 4.66 × 0.43 mm, 0.35 mm pin pitch

1.3 Block Diagram

Figure 1-1 illustrates the block diagram of S1SBP6A.

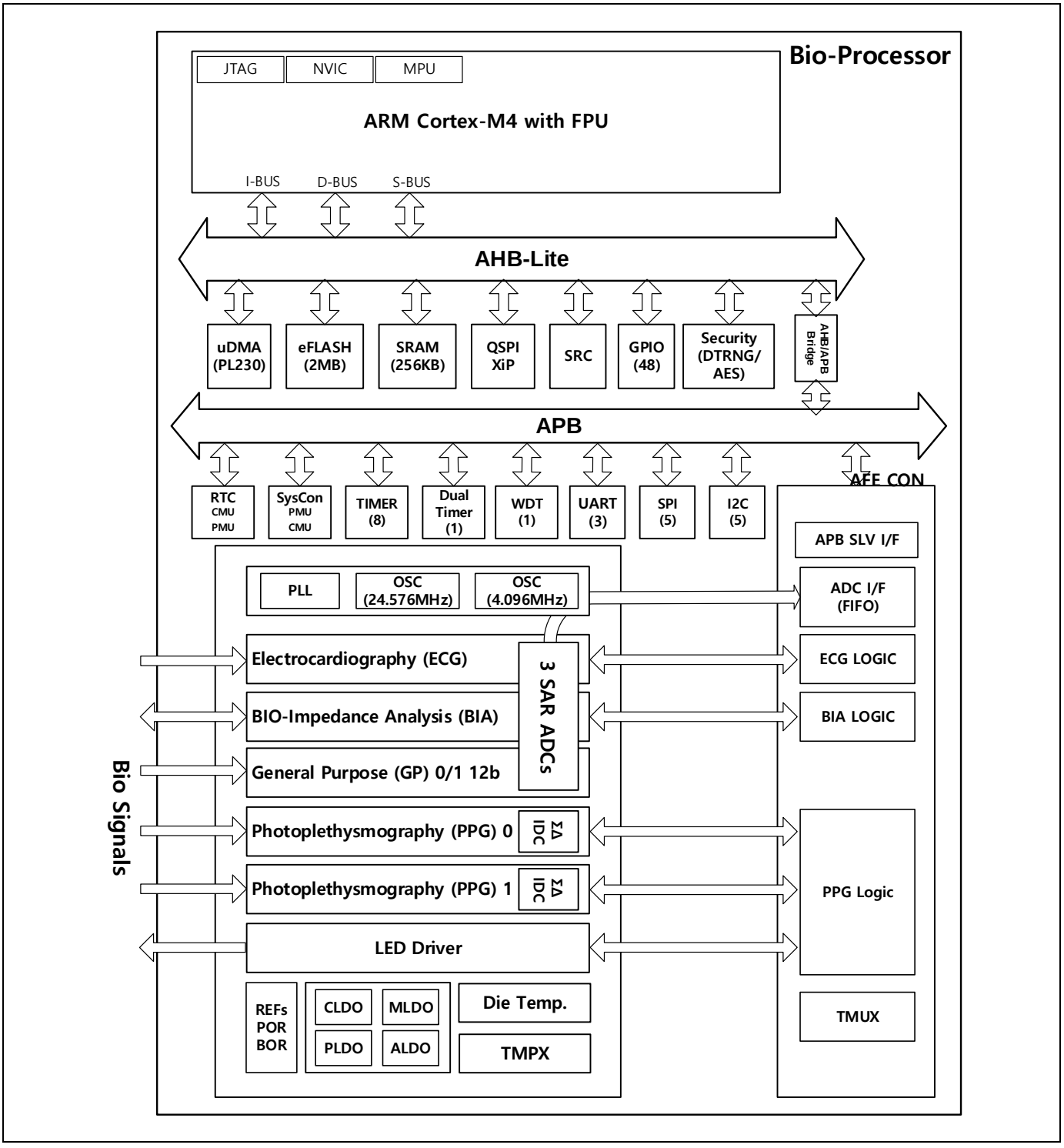

Figure 1-1 Block Diagram of S1SBP6A

2 Operating Conditions and Electrical Characteristics

This chapter includes the following sections:

- Overview
- Absolute maximum ratings
- Recommended operating conditions
- Electrical characteristics of MCU
- Electrical characteristics of AFE
- Electrical characteristics of PMIPs

2.1 Overview

This chapter describes the operating conditions and electrical specifications of digital blocks and Analog Front Ends (AFEs) implemented in S1SBP6A. These specifications are preliminary and are the results of simulation at 25 °C. These are subject to change.

2.2 Absolute Maximum Ratings

Table 2-1 describes the absolute maximum ratings.

Table 2-1 Absolute Maximum Ratings

Parameter	Value	Unit
Analog Power to Analog Ground	–0.3 to 3.3	V
Analog Ground to Digital Ground	–0.3 to 0.3	V
Electrostatic Discharge Ratings: Human Body Model (HBM)	–7.0 to 7.0	kV
Electrostatic Discharge Ratings: Charged Device Model (CDM)	–500 to 500	V
Storage Temperature: Tstg	-45 to 100	°C

NOTE: These ratings are associated only with stress. It does not imply any functional operation of the condition described in Section *2.2 Absolute Maximum Ratings*. Exposure to the absolute maximum rated conditions for long duration affects the reliability of the device.

2.3 Recommended Operating Conditions

Table 2-2 describes the recommended operating conditions.

Table 2-2 Recommended Operating Conditions

Parameter		Min.	Typ.	Max.	Unit
Analog Supply Voltage of S1SBP6A	AVDD33A	2.7	3	3.3	V
Analog Supply Voltage for Built-in LDOs	AVDD33	2.7	3	3.3	V
LED Driver Supply Voltage	AVDD33_LED	2.7	3	3.3	V
Analog Ground	AVSS33	–	0	–	V
LED Driver Ground	AVSS33_LED	–	0	–	V
Digital Supply Voltage	DVDD33	1.65	3	3.6	V
Digital Ground	DVSS33	–	0	–	V
Operating Ambient Temperature	Ta	–25	–	80	°C

NOTE: External noise filtering is recommended to supply voltage through AVDD33A.

2.4 Electrical Characteristics of MCU

Table 2-3 describes the electrical characteristics of MCU.

Table 2-3 Electrical Characteristics of MCU

Parameters		Conditions	Min.	Typ.	Max.	Unit
Clock Frequency	AHB clock	When PLL is used	–	–	102.4	MHz
	APB clock	When PLL is used	–	–	102.4	MHz
	DSP clock	When PLL is used	–	–	70	MHz
	AFE control clock	When one of External 4.096 MHz crystal input, HSOSC, and LSOSC is used.	–	4.096	–	MHz
	RTC clock	External 32.768 kHz crystal input	–	32.768	–	kHz
Current Consumption	LPM0	For more information, refer to *Table 4-11*	–	26.9	–	μA
	LPM1	For more information, refer to *Table 4-11*	–	246.4	–	μA
	LPM2	For more information, refer to *Table 4-11*	–	378.6	–	μA
	LPM3	For more information, refer to *Table 4-11*	–	461.0	–	μA
	LPM4	For more information, refer to *Table 4-11*	–	581.6	–	μA

2.5 Electrical Characteristics of AFE

2.5.1 ECG

Table 2-4 describes the electrical characteristics of ECG.

Table 2-4 Electrical Characteristics of ECG

Parameter	Condition	Min.	Typ.	Max.	Unit
Max. Differential Input	–	–	10	–	mV_{p-p}
Common-Mode Input	–	–	0.55	–	V
Max. Differential DC Offset	–	0	–	AVDD 33A	V
Gain of IA	–	–	100	–	V/V
Gain of PGA	Gain variation (± 20 %)	1	–	6	V/V
Total Channel Gain	Gain of IA × Gain of PGA	100	–	600	V/V
Bandwidth (LPF)	–	75	–	250	Hz
Bandwidth (HPF)	–	–	0.5	–	Hz
Input Impedance	Measured at 60 Hz	–	100	–	MΩ
CMRR @ 60 Hz	Without input source mismatch	–	80	–	dB
Input Noise	Measured at 0.5 - 250 Hz	–	3.5	–	μV_{rms}
ADC Resolution	–	–	12	–	bit
ADC Sampling Speed	–	1	–	8	kHz
ADC Reference Voltage	–	–	1.1	–	V
Total Harmonic Distortion (THD)	Measured at 10 mV_{p-p} input	–	–	1	%
Body Bias Drivability	–	–	10	–	μA
Power Consumption	Includes body bias voltage source and excludes LDO power consumption	–	42	–	μW

NOTE: The performances are not including non-ideal effects of electrodes.

2.5.2 PPG

Table 2-5 describes the electrical characteristics of PPG.

Table 2-5 Electrical Characteristics of PPG

Parameter		Condition	Min.	Typ.	Max.	Unit
LED Driver	# of LED Driver	2 for RED/IR 2 for GREEN	–	4	–	ea
	LED Driver Output Voltage	–	1.2	–	–	V
	Operating Current	–	–	523	–	μA
	LED Driving Current Range	0.78 mA/step, Max. current 0.39 mA/step, Max. current	–	100 50	–	mA mA
	LED Driving Current Resolution	–	–	7	–	bit
	LED Pulse Repetition Rate	–	100	–	1000	Hz
	LED On Time	–	50	–	–	μs
PPG Receiver	# of Photo Diode (PD)	–	–	2	–	ea
	PD Capacitance	–	–	–	100	pF
	DCC DAC Current	–	–16	–	16	μA
	DCC Resolution	–	–	6	–	bit
	Trans-Impedance	–	10	–	2000	kΩ
	Input Noise	Includes DCC (16 μA output) Includes DCC (8 μA output) Excludes DCC (Rf = 250 kΩ, Cf = 6 pF)	–	200 100 30	–	pA_{rms}
	Receiver SNR	BW: 20 Hz TIA: 500 kΩ 50 % FS output, LED pulse repetition: 1 kHz Excludes DC cancellation	–	90	–	dBFS
	Data Rate	–	100	–	1000	Hz
	ADC Resolution	–	–	24	–	bit
	ADC Sampling speed	–	–	2.048	–	MHz
	Power Consumption	Pulse repetition:1 kSPS LED on time: 100 μs, Per 1ch. 10 % active power control For more information, refer to *Figure 5-8*	–	600	–	μW

NOTE: The performances are not including non-ideal effects of LEDs and PDs.

2.5.3 BIA

Table 2-6 describes the electrical characteristics of BIA.

Table 2-6 Electrical Characteristics of BIA

Parameter		Condition	Min.	Typ.	Max.	Unit
TX	DAC Resolution	–	–	6	–	bit
	DAC FS Voltage	Common-mode voltage = 0.55 V	0.3	0.5	0.6	V_{p-p}
	Driving Current	Ext. resistor = 0 kΩ Int. resistor = 1.67 kΩ	–	105	–	μA_{rms}
		Ext. resistor = 6.8 kΩ Int. resistor = 1.67 kΩ	–	20	–	μA_{rms}
	DAC Sampling Speed	–	–	–	4	MHz
	Filter Bandwidth	–	125	–	2000	kHz
	Sine-Wave Frequency	–	1	–	1000	kHz
	Operating Current	Driving current 105 μA_{rms}	–	700	–	μA
RX	Frequency range of injection	VDD = 1.1 V	1	-	1000	kHz
	Gain	PGA	0.5	–	12	V/V
	Bandwidth	Int. resistor = 5 kΩ Ext. capacitor = 4.7 μF	–	6.7	–	Hz
	Input Impedance	–	–	500	–	kΩ
	Nonlinearity	500 Ω - 2 kΩ	–	1	–	%
	Operating Current	–	–	400	–	μA
	ADC Resolution	–	–	12	–	bit
	ADC Sampling Speed	–	1	–	8	kHz
	ADC Reference Voltage	–	–	1.1	–	V

NOTE: The performances are not including non-ideal effects of electrodes.

2.5.4 GP Analog Interfaces

2.5.4.1 12b GP Analog Readouts

Table 2-7 describes the analog readouts of 12b GP.

Table 2-7 Electrical Characteristics of 12b GP Analog Readouts

Parameter		Condition	Min.	Typ.	Max.	Unit
Trans-Impedance Amplifier (TIA)	Trans-Impedance (TI)	For more information, refer to *Table 5-5*.	0.6	–	10.4	MΩ
	Bandwidth		1	–	35.3	kHz
	Input Current Range	1.4 V_{p-p}/TI	0.1	–	1.65	μA_{rms}
	Signal-to-Noise Ratio	Input Current = 0.125 μA, TI = 10.4 MΩ	–	58	–	dB
Variable Gain Amplifier (VGA)	Gain	For more information, refer to *Table 5-6*.	2	–	16	V/V
	Bandwidth		1	–	2	kHz
	Input Voltage Range	1.4 V_{p-p}/Gain	–	–	700	mV_{p-p}
	Signal-to-Noise Ratio	Input = 0.04 V_{p-p}, Gain = 16	–	56	–	dB
Low Pass Filter (LPF)	Bandwidth	Differential-mode For more information, refer to *Table 5-7*	1	–	16.3	kHz
Voltage Attenuator	Gain (NOTE)	For more information, refer to *Figure 5-19*	–	0.2	–	V/V
	Int. Attenuator Resistor	–	–	100	–	kΩ
	Input Voltage Range	–	–	–	1.4	V_{p-p}
Die Temp.	Temperature Range		10	–	85	°C
Total Harmonic Distortion (THD)		–3 dB FS, GP Analog Full Path	–	–	1	%
ADC Reference		–	–	1.1	–	V
ADC Speed		–	1	–	8	kHz
ADC Resolution		–	–	12	–	bit
Signal-to-Noise Ratio		Fs = 8 kSPS Fin = 137 Hz	–	65	–	dB
Signal-to-Noise and Distortion Ratio		Fs = 8 kSPS Fin = 137 Hz	–	64	–	dB
Spurious-Free Dynamic Range		Fs = 8 kSPS Fin = 137 Hz	–	71.2	–	dB
Operating Current		GP Analog + ADC	–	42	–	μA

NOTE: Rext = 200 kΩ Gain is determined depending on the value of Rext.

2.6 Electrical Characteristics of PMIPs and Clock Generators

2.6.1 PMIP

Table 2-8 describes the electrical characteristics of PMIPs.

Table 2-8 Electrical Characteristics of PMIPs

Parameter		Condition	Min.	Typ.	Max.	Unit
Input Voltage		–	2.7	–	3.3	V
Output Voltage	ALDO	–	–	1.1	–	V
	PLDO	–	–	1.1	–	V
	MLDO	–	–	1.1	–	V
	CLDO	–	–	1.1	–	V
Max. Load Current	ALDO	–	–	20	–	mA
	PLDO	–	–	10	–	mA
	MLDO	–	–	30	–	mA
	CLDO	–	–	40	–	mA
Line Regulation	ALDO	–	–	20	–	mV/V
	PLDO	–	–	25	–	mV/V
	MLDO	–	–	10	–	mV/V
	CLDO	–	–	10	–	mV/V
Load Regulation	ALDO	–	–	20	–	mV/A
	PLDO	–	–	20	–	mV/A
	MLDO	–	–	10	–	mV/A
	CLDO	–	–	10	–	mV/A
Standby Current Consumption	ALDO	–	–	4	–	μA
	PLDO	–	–	2	–	μA
	MLDO	–	–	7	–	μA
	CLDO	–	–	7	–	μA
Start-up Time	ALDO	–	–	0.1	–	ms
	PLDO	–	–	0.1	–	ms
	MLDO	–	–	0.1	–	ms
	CLDO	–	–	0.1	–	ms
Threshold Voltage	POR	–	1.52	–	1.62	V
	BOR	–	2.6	–	2.7	V
	Operating Current	–	–	7.5	–	μA

2.6.2 Clock Generators

- **Phase-Locked Loop**

Table 2-9 describes the electrical characteristics of Phase-Locked Loop.

Table 2-9 Electrical Characteristics of Phase-Locked Loop

Parameter	Condition	Min.	Typ.	Max.	Unit
Operating Current	PLDO_OUT = 1.1 V, 50 MHz, 25 °C	–	1.5	–	mA
Power Down Current	RESETB = 0, 25 °C	–	0.5	–	μA
Input Frequency	–	4	16	100	MHz
Reference Frequency	–	2	4	10	MHz
PLL Output Frequency	4.096 MHz Crystal Input	–	102.4	–	MHz
VCO Output Frequency	–	100	–	200	MHz
Duty Ratio	–	40	–	60	%
Lock Time (1)	–	–	–	200	cycles
Period Jitter	–	–	–	± 1.5 (2)	%
Frequency Setting Range	–	0.71	–	1.64	MHz

NOTE:

1 1 cycle = 1/(Reference Frequency) = 1/(Input Frequency/pre-divider value)

2 ± 1.5 of VCO period

- **High Speed Oscillator**

Table 2-10 describes the electrical characteristics of High Speed Oscillator.

Table 2-10 Electrical Characteristics of High Speed Oscillator

Parameter	Condition	Min.	Typ.	Max.	Unit
Operating Current	PLDO_OUT = 1.1 V, 25 °C	–	12	–	μA
Power Down Current	RESETB = 0, 25 °C	–	–	–	μA
Short-Term Period Jitter	–	–	–	15 %	Period
Output Frequency by CS (NOTE)	Under all PVT variation	–2 %	24.576	+2 %	MHz
Duty Ratio by CS (NOTE)	–	20	50	80	%
Lock Time by CS (NOTE)	–	–	–	300	μs

NOTE: CS: Calibration Scheme. Oscillator frequency can be calibrated using external 32.768 kHz clock.

- **Low Speed Oscillator**

Table 2-11 describes the electrical characteristics of **Low-Speed Oscillator.**

Table 2-11 Electrical Characteristics of Low-Speed Oscillator

Parameter	Condition	Min.	Typ.	Max.	Unit
Operating Current	PLDO_OUT = 1.1 V, 25 °C	–	8	–	μA
Power Down Current	RESETB = 0, 25 °C	–	–	–	μA
Short-term Period Jitter	–	–	–	15 %	Period
Output Frequency by CS (NOTE)	Under all PVT variation	–2 %	4.096	+2 %	MHz
Duty Ratio by CS (NOTE)	–	20	50	80	%
Lock Time by CS (NOTE)	–	–	–	300	μs

NOTE: CS: Calibration Scheme. Oscillator frequency can be calibrated using external 32.768 kHz clock.

3 Ball Map and Pin Description

This chapter includes the following sections:

- Overview
- Ball map
- Pin description

3.1 Overview

This chapter describes S1SBP6A ball map and signal pins.

3.2 Ball Map

Figure 3-1 illustrates the ball map of S1SBP6A device.

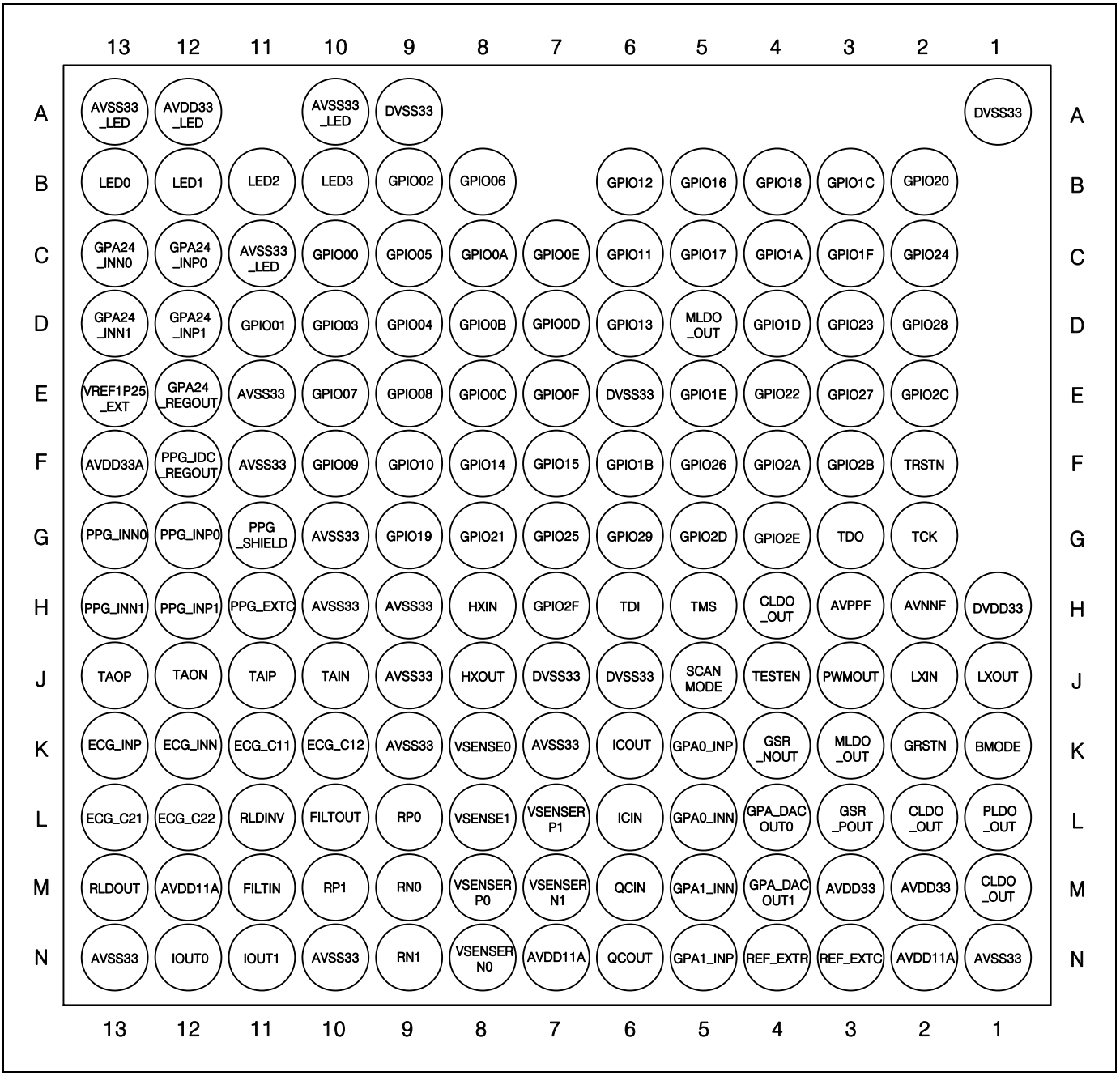

Figure 3-1 Ball Map of S1SBP6A

3.3 Pin Description

Table 3-1 describes the pin assignment.

Table 3-1 Pin Description of S1SBP6A

No.	Ball	Pin	Description	I/O
1	B12	LED1	LED Driver1 Output (tolerable up to 5 V)	AIO
2	B13	LED0	LED Driver0 Output (tolerable up to 5 V)	AIO
3	C12	GPA24_INP0	Positive Analog Signal Input for GSR (24b)	AI
4	C13	GPA24_INN0	Negative Analog Signal Input for GSR (24b)	AI
5	D12	GPA24_INP1	No use	AI
6	D13	GPA24_INN1	No use	NC
7	C11	AVSS33	Analog Ground	AG
8	E13	VREF1P25_EXT	External 1.25 V Reference Voltage Input	AI
9	E12	GPA24_REGOUT	GSR (24b) Regulator Output	AO
10	F12	PPG_IDC_REGOUT	IDC (24b) Regulator Output	AO
11	F13	AVDD33A	3 V Analog Power Supply	AP
12	G12	PPG_INP0	Photo Diode Cathode Input0	AI
13	G13	PPG_INN0	Photo Diode Anode Input0	AI
14	G11	PPG_SHIELD	Photo Diode Shied Voltage Output	AO
15	H11	PPG_EXTC	External Capacitor for DCC Noise Filtering	AI
16	H13	PPG_INN1	Photo Diode Anode Input0	AI
17	H12	PPG_INP1	Photo Diode Cathode Input0	AI
18	J11	TAIP	External Positive Input for Analog Buffer to Monitor Internal Analog Signal	AI
19	J13	TAOP	Positive Analog Buffer Output	AO
20	J12	TAON	Negative Analog Buffer Output	AO
21	J10	TAIN	External Negative Input for Analog Buffer to Monitor Internal Analog Signal	AI
22	K12	ECG_INN	Negative ECG Signal Input	AI
23	K13	ECG_INP	Positive ECG Signal Input	AI
24	K11	ECG_C11	External Capacitor Port1 for Negative Input of HPF2 in ECG Readout	AIO
25	K10	ECG_C12	External Capacitor Port2 for Negative Input of HPF2 in ECG Readout	AIO
26	L13	ECG_C21	External Capacitor Port1 for Positive Input of HPF2 in ECG Readout	AIO
27	L12	ECG_C22	External Capacitor Port2 for Positive Input of HPF2 in ECG Readout	AIO
28	L11	RLDINV	Negative Input of ECG Electrode Driver for Body Bias	AI
29	M13	RLDOUT	Output of ECG Electrode Driver for Body Bias	AO
30	M12	AVDD11A	ALDO Output (1.1 V) for ECG, BIA, GPA0/1, 12b ADC, 10b GP DAC	AO
31	L10	FILTOUT	BIA DAC Filter Output	AO
32	M11	FILTIN	BIA Current Converter Input	AI
33	N12	IOUT0	BIA Current Driver Output0	AO

No.	Ball	Pin	Description	I/O
34	N11	IOUT1	BIA Current Driver Output1	AO
35	L9	RP0	BIA Calibration Resistor0 Positive Port	AIO
36	M10	RP1	BIA Calibration Resistor1 Positive Port	AIO
37	M9	RN0	BIA Calibration Resistor0 Negative Port	AIO
38	N9	RN1	BIA Calibration Resistor1 Negative Port	AIO
39	N10	AVSS33	Analog Ground	AG
40	K8	VSENSE0	BIA Differential Amplifier Input0 for Voltage Sensing	AI
41	L8	VSENSE1	BIA Differential Amplifier Input1 for Voltage Sensing	AI
42	M8	VSENSERP0	BIA Differential Amplifier Input0 for Voltage Sensing from Resistor0	AI
43	L7	VSENSERP1	BIA Differential Amplifier Input0 for Voltage Sensing from Resistor1	AI
44	N8	VSENSERN0	BIA Differential Amplifier Input1 for Voltage Sensing from Resistor0	AI
45	M7	VSENSERN1	BIA Differential Amplifier Input1 for Voltage Sensing from Resistor1	AI
46	N7	AVDD11A	ALDO Output (1.1 V) for ECG, BIA, GPA0/1, 12b ADC, 10b GP DAC	AO
47	K6	ICOUT	I Channel Demodulator Low Pass Filter, Connect 4.7 μF between ICOUT and Ground	AIO
48	L6	ICIN	I Channel Demodulator Low Pass Filter, Connect 4.7 μF between ICIN and Ground	AI
49	N6	QCOUT	Q Channel Demodulator Low Pass Filter, Connect 4.7 μF between QCOUT and Ground	AIO
50	M6	QCIN	Q Channel Demodulator Low Pass Filter, Connect 4.7 μF between QCIN and Ground	AI
51	K5	GPA0_INP	GP Analog0 Positive Analog Signal Input	AI
52	L5	GPA0_INN	GP Analog0 Negative Analog Signal Input	AI
53	N5	GPA1_INP	GP Analog1 Positive Analog Signal Input	AI
54	M5	GPA1_INN	GP Analog1 Negative Analog Signal Input	AI
55	L4	GPA_DACOUT0	No use	AO
56	M4	GPA_DACOUT1	No use	AO
57	K4	GSR_NOUT	Negative GSR Electrode Connecting Pin	AIO
58	L3	GSR_POUT	Positive GSR Electrode Connecting Pin	AIO
59	N4	REF_EXTR	External Resistor (75 kΩ) for On-Chip Bias Generation	AIO
60	N3	REF_EXTC	External Noise Filtering Capacitor (4.7 μF) for On-Chip 1.25 V Reference	AIO
61	N2	AVDD11A	ALDO Output (1.1 V) for ECG, BIA, GPA0/1, 12b ADC, 10b GP DAC	AO
62	M3	AVDD33	3 V Analog Power Supply for LDOs	AP
63	N1	AVSS33	Analog Ground	AG
64	M2	AVDD33	3 V Analog Power Supply for LDOs	AG
65	M1	CLDO_OUT	LDO Output for MCU and Slim-SRP	AO
66	L2	CLDO_OUT	LDO Output for MCU and Slim-SRP	AO
67	K3	MLDO_OUT	LDO Output for SRAM and Flash Memory	AO

No.	Ball	Pin	Description	I/O
68	L1	PLDO_OUT	LDO Output for PLL and Oscillators	AO
69	K2	GRSTN	Global Reset	DIO
70	K1	BMODE	At Start Up (0: Embedded Flash Boot Mode, 1: External Serial, Flash Boot Mode), After Start Up (Wakeup Source)	DIO
71	J5	SCANMODE	Scan Mode Enable	DIO
72	J4	TESTEN	Test Mode Enable	DIO
73	J3	PWMOUT	PWM Out	DIO
74	J1	LXOUT	32.768 kHz Crystal Output	DIO
75	J2	LXIN	32.768 kHz Crystal Input	DIO
76	J6	DVSS33	Digital Ground	DG
77	H1	DVDD33	Digital Power	DP
78	J8	HXOUT	4.096 MHz Crystal Output	DIO
79	H8	HXIN	4.096 MHz Crystal Input	DIO
80	H2	AVNNF	Negative High Voltage Forcing and Monitoring Port (–9 V ~ 0 V)	AIO
81	H3	AVPPF	Positive High Voltage Forcing and Monitoring Port (0 V ~ 12 V)	AIO
82	H4	CLDO_OUT	LDO Output for MCU and Slim-SRP	AO
83	J7	DVSS33	Digital Ground	DG
84	G2	TCK	Test Clock	DIO
85	H5	TMS	Test Mode Selection	DIO
86	H6	TDI	Test Data Input	DIO
87	G3	TDO	Test Data Output	DIO
88	F2	TRSTN	TRSTN (Active Low)	DIO
89	H7	GPIO2F	GPIO2F/QSPI_CLK	DIO
90	G4	GPIO2E	GPIO2E/QSPI_CS	DIO
91	G5	GPIO2D	GPIO2D/QSPI_SI	DIO
92	E2	GPIO2C	GPIO2C/QSPI_SO	DIO
93	F3	GPIO2B	GPIO2B/QSPI_WP	DIO
94	F4	GPIO2A	GPIO2A/Timer0_EXT/QSPI_HLD	DIO
95	G6	GPIO29	GPIO29/I2C0_SDA	DIO
96	D2	GPIO28	GPIO28/I2C0_SCL	DIO
97	E3	GPIO27	GPIO27/UART0_RTSN	DIO
98	F5	GPIO26	GPIO26/UART0_CTSN	DIO
99	G7	GPIO25	GPIO25/UART0_RX	DIO
100	C2	GPIO24	GPIO24/UART0_TX	DIO
101	D3	GPIO23	GPIO23/SPI0_MISO	DIO
102	E4	GPIO22	GPIO22/SPI0_MOSI	DIO
103	A1	DVSS33	Digital Ground	DG

No.	Ball	Pin	Description	I/O
104	G8	GPIO21	GPIO21/SPI0_CSN	DIO
105	B2	GPIO20	GPIO20/SPI0_CLK	DIO
106	C3	GPIO1F	GPIO1F/I2C4_SDA	DIO
107	E5	GPIO1E	GPIO1E/I2C4_SCL	DIO
108	D4	GPIO1D	GPIO1D/I2C3_SDA	DIO
109	B3	GPIO1C	GPIO1C/I2C3_SCL	DIO
110	F6	GPIO1B	GPIO1B/I2C2_SDA	DIO
111	C4	GPIO1A	GPIO1A/I2C2_SCL	DIO
112	G9	GPIO19	GPIO19/I2C1_SDA	DIO
113	B4	GPIO18	GPIO18/I2C1_SCL	DIO
114	D5	MLDO_OUT	LDO Output for SRAM and Flash Memory	AO
115	E6	DVSS33	Digital Ground	DG
116	C5	GPIO17	GPIO17/UART2_RTSN/PWMOUT	DIO
117	B5	GPIO16	GPIO16/UART2_CTSN/32.768 kHz	DIO
118	F7	GPIO15	GPIO15/UART2_RX	DIO
119	F8	GPIO14	GPIO14/UART2_TX	DIO
120	D6	GPIO13	GPIO13/UART1_RTSN/PTimer_EXT	DIO
121	B6	GPIO12	GPIO12/UART1_CTSN/Timer6_EXT	DIO
122	C6	GPIO11	GPIO11/UART1_RX	DIO
123	F9	GPIO10	GPIO10/UART1_TX/Timer5_EXT	DIO
124	E7	GPIO0F	GPIO0F/SPI4_MISO/Timer4_EXT	DIO
125	C7	GPIO0E	GPIO0E/SPI4_MOSI/Timer3_EXT	DIO
126	D7	GPIO0D	GPIO0D/SPI4_CSN/Timer2_EXT	DIO
127	E8	GPIO0C	GPIO0C/SPI4_CLK/Timer1_EXT	DIO
128	D8	GPIO0B	GPIO0B/SPI3_MISO	DIO
129	C8	GPIO0A	GPIO0A/SPI3_MOSI	DIO
130	F10	GPIO09	GPIO09/SPI3_CSN	DIO
131	E9	GPIO08	GPIO08/SPI3_CLK	DIO
132	E10	GPIO07	GPIO07/SPI2_MISO	DIO
133	B8	GPIO06	GPIO06/SPI2_MOSI	DIO
134	C9	GPIO05	GPIO05/SPI2_CSN	DIO
135	D9	GPIO04	GPIO04/SPI2_CLK	DIO
136	D10	GPIO03	GPIO03/SPI1_MISO	DIO
137	B9	GPIO02	GPIO02/SPI1_MOSI	DIO
138	D11	GPIO01	GPIO01/SPI1_CSN	DIO
139	C10	GPIO00	GPIO00/SPI1_CLK	DIO
140	A9	DVSS33	Digital Ground	DG

No.	Ball	Pin	Description	I/O
141	A10	AVSS33_LED	Ground for LED Driver	AG
142	B10	LED3	LED Driver3 Output (tolerable up to 3 V)	AIO
143	B11	LED2	LED Driver2 Output (tolerable up to 3 V)	AIO
144	A13	AVSS33_LED	Ground for LED Driver	AG
145	A12	AVDD33_LED	3 V Analog Power Supply for LED Drivers	AP
146	E11	AVSS33	Analog Ground	AG
147	F11	AVSS33	Analog Ground	AG
148	G10	AVSS33	Analog Ground	AG
149	H10	AVSS33	Analog Ground	AG
150	H9	AVSS33	Analog Ground	AG
151	J9	AVSS33	Analog Ground	AG
152	K9	AVSS33	Analog Ground	AG
153	K7	AVSS33	Analog Ground	AG
154	N13	AVSS33	Analog Ground	AG

NOTE: AI: Analog Input
DI: Digital Input
AO: Analog Output
DO: Digital Output
AIO: Analog Input/Output
AP: Analog Power
AG: Analog Ground
DIO: Digital Input/Output
DP: Digital Power
DG: Digital Ground
P: Power
G: Ground
NC: No Connection

4 MCU

This chapter includes the following sections:

- Overview
- Subsystems
- System control

4.1 Overview

S1SBP6A integrates MCU, DSP, and AFE circuit controllers. MCU takes master control role of S1SBP6A such as managing Operating System (OS), signal processing, interfacing with external devices, and other common tasks. MCU comprises ARM Cortex-M4 core as a main processor, 2 MB embedded Flash with 2 KB Cache, 256 KB SRAM, Security IPs, and various peripherals.

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Following are the features of MCU subsystem:

- MCU with Cortex-M4 core with FPU
- 2 MB embedded Flash with 2 KB Cache and 256 KB SRAM
- System control such as RTC, CMU, and PMU
- 32 channel μDMAC
- Three channel UARTs, five channel SPIs, five channel I2Cs, and 48 Pin GPIO (Three 16-pin GPIO ports)
- Seven Timers, one PWM Timer, one Dual-Input Timer, one Watchdog, and one RTC
- Security IPs such as AES and DTRNG
- Sample Rate Converter (SRC) as a hardware accelerator
- Serial Flash Interface with execution-in-place (XiP) capability
- JTAG/software interface for debug

4.2 Subsystems

4.2.1 Memory

Table 4-1 describes the detailed memory allocation of S1SBP6A.

Table 4-1 Memory Allocation Details

Address	Memory Map
0x70001000 - 0x7FFFFFFF	Unused
0x70000000 - 0x70000FFF	Serial Flash Interface SFRs
0x60000000 - 0x6FFFFFFF	External Serial Flash (256 MB)
0x40030000 - 0x5FFFFFFF	Unused
0x4002F000 - 0x4002FFFF	System Controller Registers
0x40025000 - 0x40025FFF	Flash SFRs
0x40024000 - 0x40024FFF	DTRNG
0x40023000 - 0x40023FFF	AES
0x40022FFF - 0x40022000	AHB GPIO 2
0x40021FFF - 0x40021000	AHB GPIO 1
0x40020FFF - 0x40020000	AHB GPIO 0
0x4001E000 - 0x4001FFFF	Unused
0x40000000 - 0x4001DFFF	APB Subsystem Peripherals
0x20040000 - 0x3FFFFFFF	Unused
0x20000000 -0x2003FFFF	Data Memory (SRAM 256 KB)
0x10000800 - 0x1FFFFFFF	Unused
0x10000000 - 0x100007FF	Flash Cache (2 KB)
0x00400000 - 0x004005FF	Flash Security Region (1.5 KB)
0x00000000 - 0x001FFFFF	Program Memory (eFlash 2 MB)

Table 4-2 describes APB-subsystem memory space allocation of S1SBP6A.

Table 4-2 APB Subsystem Memory Map

Address	Memory Map
0x4001D000 - 0x4001DFFF	SRC
0x4001C000 - 0x4001CFFF	SYSCON
0x4001B000 - 0x4001BFFF	µDMAC
0x4001A000 - 0x4001AFFF	AFE Controller
0x40019000 - 0x40019FFF	RTC
0x40018000 - 0x40018FFF	Unused
0x40017000 - 0x40017FFF	Delay Monitor
0x40016000 - 0x40016FFF	I2C4
0x40015000 - 0x40015FFF	I2C3
0x40014000 - 0x40014FFF	I2C2
0x40013000 - 0x40013FFF	I2C1
0x40012000 - 0x40012FFF	I2C0
0x40011000 - 0x40011FFF	SPI4
0x40010000 - 0x40010FFF	SPI3
0x4000F000 - 0x4000FFFF	SPI2
0x4000E000 - 0x4000EFFF	SPI1
0x4000D000 - 0x4000DFFF	SPI0
0x4000C000 - 0x4000CFFF	UART2
0x4000B000 - 0x4000BFFF	UART1
0x4000A000 - 0x4000AFFF	UART0
0x40009000 - 0x40009FFF	Watchdog
0x40008000 - 0x40008FFF	Dual Timer
0x40007000 - 0x40007FFF	PWM Timer1
0x40006000 - 0x40006FFF	PWM Timer0
0x40005000 - 0x40005FFF	Timer5
0x40004000 - 0x40004FFF	Timer4
0x40003000 - 0x40003FFF	Timer3
0x40002000 - 0x40002FFF	Timer2
0x40001000 - 0x40001FFF	Timer1
0x40000000 - 0x40000FFF	Timer0

4.2.2 Bus Architecture

Bus architecture of S1SBP6A is illustrated in *Figure 4-1*. It supports AHB-Lite protocol which is a simple subset of the full AHB specification. The Bus Matrix includes seven slave ports and two master ports. Seven slave ports are connected to three AHB masters which are µDMAC, Cortex-M4, and SRC. A bus master port of µDMAC has the highest priority of AHB occupation. Three AHB master ports of Cortex-M4, System bus, D-Code bus, and I-Code bus, have next higher priorities. System bus is connected to system components such as AHB/APB peripherals, Flash, and SRAM. I-Code bus fetches instruction and vector from code memory space and D-Code bus performs data and debug accesses to code memory space. SRC has three master bus ports such as Sample bus, Coefficient bus, and Result bus, and they have lower priorities. Two master ports of Bus Matrix are connected to Code Bus Mux and System Bus Mux.

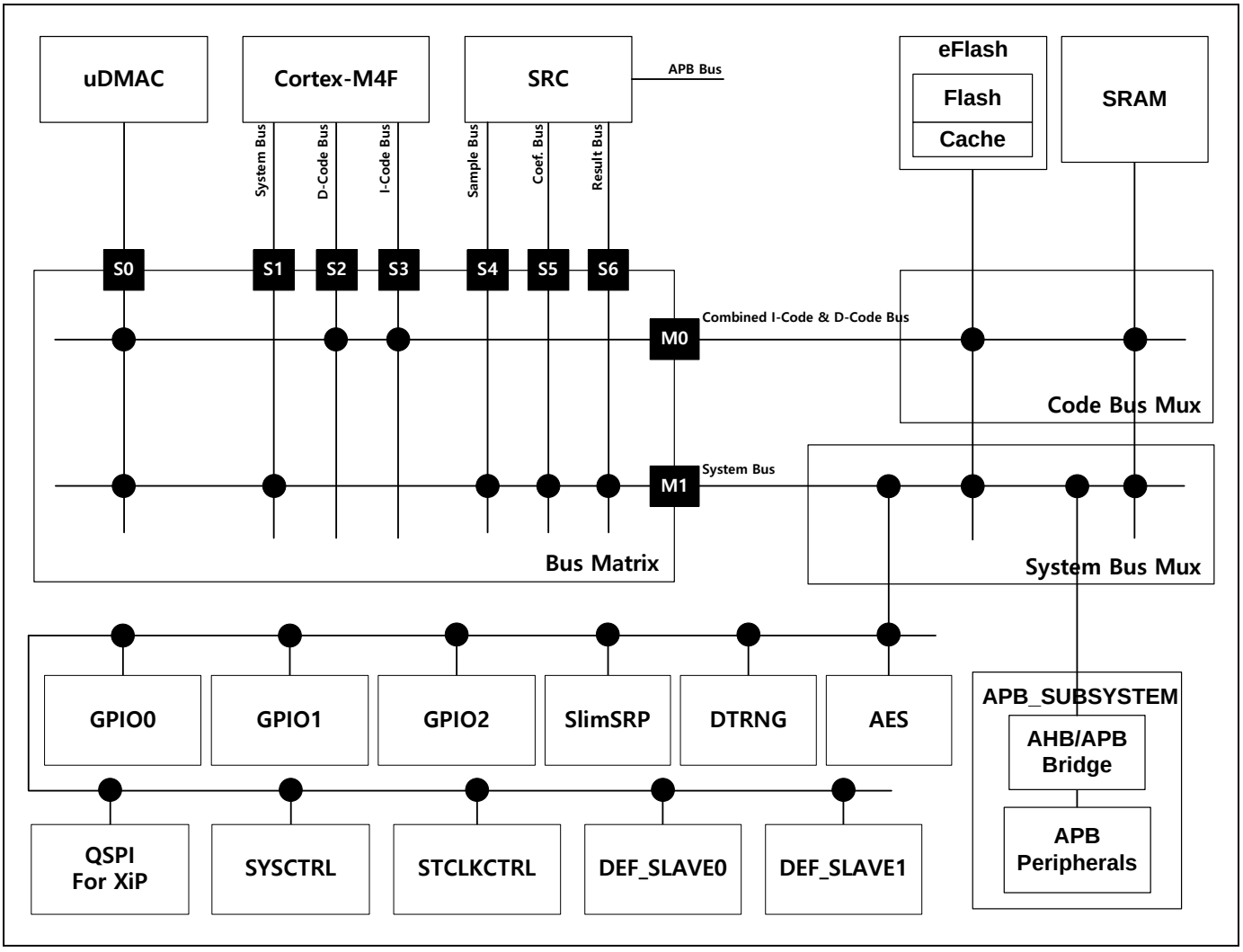


Figure 4-1 Bus Architecture

4.2.3 ARM Cortex-M4 with Floating-Point Unit (Cortex-M4F)

The processor core of S1SBP6A is ARM Cortex-M4 with Floating-Point Unit (Cortex-M4F). Cortex-M4 processor is a high performance 32-bit RISC processor with a 3-stage pipeline Harvard architecture, making it ideal for demanding embedded applications. Cortex-M4 processor implements a version of the Thumb instruction set based on Thumb-2 technology ensuring high code density and reduced program memory requirements. The instruction set of Cortex-M4 provides the exceptional performance expected of a modern 32-bit architecture with the high code density of 8-bit and 16-bit microcontrollers. *Figure 4-2* illustrates the structure of Cortex-M4F processor.

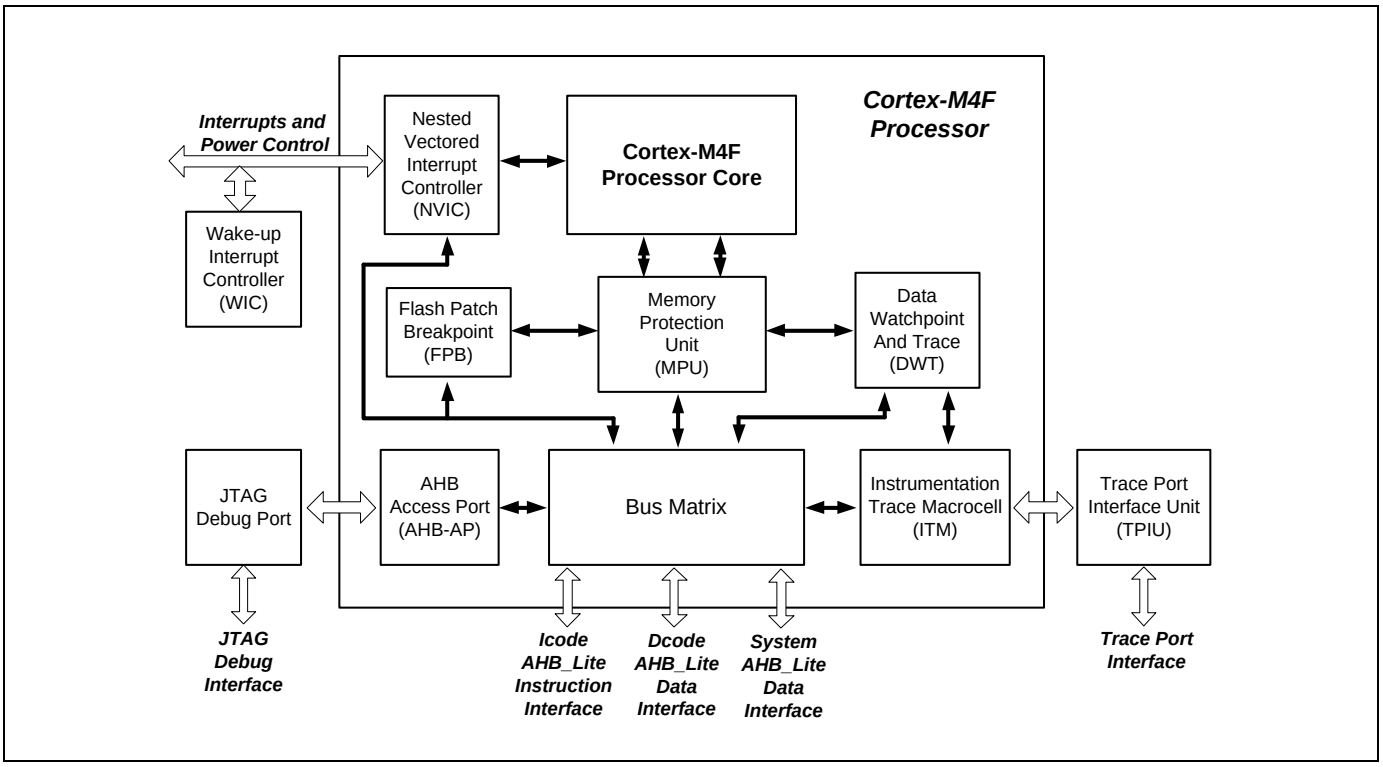


Figure 4-2 Cortex-M4F Block Diagram

Following are the features of ARM Cortex-M4F processor:

- A low gate count processor core, with low latency interrupt processing that has the following characteristics:
  - A subset of the Thumb instruction set, defined in the ARMv7-M Architecture Reference Manual
  - Banked Stack Pointer (SP)
  - Hardware integer divide instructions such as SDIV and UDIV
  - Handler and thread modes
  - Thumb and debug states
  - Support for interruptible-continued instructions such as LDM, STM, PUSH, and POP for low interrupt latency
  - Automatic processor state saving and restoration for low latency Interrupt Service Routine (ISR) entry and exit
  - Support for ARMv6 big-endian byte-invariant or little-endian accesses
  - Support for ARMv6 unaligned accesses

- Floating-Point Unit (FPU) in the Cortex-M4F processor has the following characteristics:
  - 32-bit instructions for single-precision (C float) data-processing operations
  - Combined multiply and accumulate instructions for increased precision (Fused MAC)
  - Hardware support for conversion, addition, subtraction, multiplication with optional accumulate, division, and square-root
  - Hardware support for denormals and all IEEE rounding modes
  - 32 dedicated 32-bit single precision registers, also addressable as 16 double-word registers
  - Decoupled three stage pipeline
- Nested Vectored Interrupt Controller (NVIC) closely integrated with the processor core to achieve low latency interrupt processing. Following are the supported features:
  - External interrupts, configurable from 1 to 240
  - Bits of priority, configurable from 3 to 8
  - Dynamic reprioritization of interrupts
  - Priority grouping. This enables selection of preempting interrupt levels and non-preempting interrupt levels
  - Tail-chaining and late arrival of interrupts. This enables back-to-back interrupt processing without the overhead of state saving and restoration between interrupts
  - Processor state automatically saved on interrupt entry, and restored on interrupt exit, with no instruction overhead
  - Wake-up Interrupt Controller (WIC), providing ultra-low power sleep mode support
- Memory Protection Unit (MPU). An optional MPU for memory protection has the following characteristics:
  - Eight memory regions
  - Sub Region Disable (SRD), enabling efficient use of memory regions
  - The ability to enable a background region that implements the default memory map attributes
- Following are the characteristics of bus interfaces:
  - Three AHB-Lite interfaces: I-Code, D-Code, and System Bus interfaces
  - Private Peripheral Bus (PPB) based on Advanced Peripheral Bus (APB) interface
  - Bit-band support that includes atomic bit-band write and read operations
  - Memory access alignment
  - Write buffer for buffering of write data
  - Exclusive access transfers for multiprocessor systems
- Low-cost debug solution includes the following features:
  - Debug access to all memory and registers in the system, including access to memory mapped devices, access to internal core registers when the core is halted, and access to debug control registers even while SYSRESETn is asserted.
  - Serial Wire JTAG Debug Port (SWJ-DP) debug

For more information, refer to the following link for the technical reference manual of ARM Cortex-M4 processor.

http://infocenter.arm.com/help/topic/com.arm.doc.ddi0439b/DDI0439B_cortex_m4_r0p0_trm.pdf

4.2.4 Micro Direct Memory Access Controller

S1SBP6A utilizes ARM PrimeCell Micro Direct Memory Access Controller (μDMAC) (PL230) as a Direct Memory Access Controller (DMAC). μDMAC is an AMBA compliant SoC peripheral that is developed, tested, and licensed by ARM. It is a very low gate count DMAC that is compatible with the AMBA AHB-Lite protocol.

μDMAC supports the following features:

- Compatibility with AHB-Lite for the DMA transfers
- Compatibility with APB for programming the registers
- Single AHB-Lite master for transferring data using a 32-bit address bus and 32-bit data bus
- 32 DMA channels
- Each DMA channel with dedicated handshake signals
- Each DMA channel with a programmable priority level
- Each priority level arbitrates using a fixed priority that is determined by the DMA channel number
- Multiple transfer types:
  - Memory-to-Memory
  - Memory-to-Peripheral
  - Peripheral-to-Memory
- Multiple DMA cycle types
- Multiple DMA transfer data widths
- Access to primary, alternate, and channel control data structure of each DMA channel
- Little-endian format for storing all channel control data in system memory
- DMA transfers using the single AHB-Lite burst type
- Equal destination data width to the source data width
- Programmable number of transfers in a single DMA cycle from 1 to 1024
- Greater transfer address increment than the data width
- Single output to indicate when an ERROR condition occurs on the AHB bus

Table 4-3 describes the DMA channel assignment.

Table 4-3 DMA Channel Assignment

DMA Channel	Single Request	Request
0	SPI RX (0-4)	–
1	SPI TX (0-4)	–
2	SPI RX (0-4)	–
3	SPI TX (0-4)	–
4	SPI RX (0-4)	–
5	SPI TX (0-4)	–
6	SPI RX (0-4)	–
7	SPI TX (0-4)	–

DMA Channel	Single Request	Request
8	AFE FIFO6	AFE FIFO6
9	AFE FIFO7	AFE FIFO7
10	I2C RX (0-4)	–
11	I2C TX (0-4)	–
12	I2C RX (0-4)	–
13	I2C TX (0-4)	–
14	I2C RX (0-4)	–
15	I2C TX (0-4)	–
16	I2C RX (0-4)	–
17	I2C TX (0-4)	–
18	AFE FIFO08	AFE FIFO08
19	S/W	S/W
20	UART0 RX	UART0 RX
21	UART0 TX	UART0 TX
22	UART1 RX	UART1 RX
23	UART1 TX	UART1 TX
24	UART2 RX	UART2 RX
25	UART2 TX	UART2 TX
26	AFE FIFO0	AFE FIFO0
27	AFE FIFO1	AFE FIFO1
28	AFE FIFO2	AFE FIFO2
29	AFE FIFO3	AFE FIFO3
30	AFE FIFO4	AFE FIFO4
31	AFE FIFO5	AFE FIFO5

Use the following link to access the final version of µDMAC technical reference manual.

http://infocenter.arm.com/help/topic/com.arm.doc.ddi0417a/DDI0417A_udmac_pl230_r0p0_trm.pdf

4.2.4.1 Register Description

This section describes the register map information and its associated registers.

4.2.4.1.1 Register Map Summary

- Base Address: 0x4001_B000

Register	Offset	Description	Reset Value
DMA_STATUS	0x0000	DMA Status	0x001F_0000
DMA_CFG	0x0004	DMA Configuration	0x0000_0000
CTRL_BASE_PTR	0x0008	Channel Control Database Pointer	0x0000_0000
ALT_CTRL_BASE_PTR	0x000C	Channel Alternate Control Database Pointer	0x0000_0000
DMA_WAITONREQ_STATUS	0x0010	Channel Wait On Request Status	0x0000_0000
CHNL_SW_REQUEST	0x0014	Channel Software Request	0x0000_0000
CHNL_USEBURST_SET	0x0018	Channel Useburst Set	0x0000_0000
CHNL_USEBURST_CLR	0x001C	Channel Useburst Clear	0x0000_0000
CHNL_REQ_MASK_SET	0x0020	Channel Request Mask Set	0x0000_0000
CHNL_REQ_MASK_CLR	0x0024	Channel Request Mask Clear	0x0000_0000
CHNL_ENABLE_SET	0x0028	Channel Enable Set	0x0000_0000
CHNL_ENABLE_CLR	0x002C	Channel Enable Clear	0x0000_0000
CHNL_PRI_ALT_SET	0x0030	Channel Primary-Alternate Set	0x0000_0000
CHNL_PRI_ALT_CLR	0x0034	Channel Primary-Alternate Clear	0x0000_0000
CHNL_PRIORITY_SET	0x0038	Channel Priority Set	0x0000_0000
CHNL_PRIORITY_CLR	0x003C	Channel Priority Clear	0x0000_0000
ERR_CLR	0x004C	Bus Error Clear	0x0000_0000
DMA_MUX	0x0050	DMA Channel Mux within I2C and SPI Peris	0x32103210
DMA_NOT_MUX	0x0054	DMA Channel not Muxed within I2C and SPI Peris	0x00000044
DMA_REQ_GATE	0x0058	DMA Request Gating Enable	0xFFFFFFFF
PERIPH_ID_4	0x0FD0	Peripheral Identification 4	0x0000_0004
PERIPH_ID_0	0x0FE0	Peripheral Identification 0	0x0000_0030
PERIPH_ID_1	0x0FE4	Peripheral Identification 1	0x0000_00B2
PERIPH_ID_2	0x0FE8	Peripheral Identification 2	0x0000_000B
PERIPH_ID_3	0x0FEC	Peripheral Identification 3	0x0000_0000
PCELL_ID_0	0x0FF0	PrimeCell Identification 0	0x0000_000D
PCELL_ID_1	0x0FF4	PrimeCell Identification 1	0x0000_00F0
PCELL_ID_2	0x0FF8	PrimeCell Identification 2	0x0000_0005
PCELL_ID_3	0x0FFC	PrimeCell Identification 3	0x0000_00B1

NOTE: If reserved or empty addresses in the register map are changed, S1SBP6A cannot guarantee normal operation.

4.2.4.1.1.1 DMA_STATUS

- Base Address: 0x4001_B000
- Address = Base Address + 0x0000, Reset Value = 0x001F_0000

Name	Bit	Type	Description	Reset Value
TEST_STATUS	[31:28]	R	Configure the controller to reduce the gate count. Read as: 0x0 = Controller does not include the integration test logic 0x1 = Controller includes the integration test logic 0x2-0xF = Undefined	0x0000_0000
CHNLS_MINUS1	[20:16]	R	Number of available DMA channels minus one. For example: b00000 = Controller configured to use 1 DMA channel b00001 = Controller configured to use 2 DMA channels b00010 = Controller configured to use 3 DMA channels … b11111 = Controller configured to use 32 DMA channels	0x0000_001F
STATE	[7:4]	R	Current state of the control state machine. State can be one of the following: b0000 = Idle b0001 = Reading the channel controller data b0010 = Reading the source data end pointer b0011 = Reading the destination data end pointer b0100 = Reading the source data b0101 = Writing the destination data b0110 = Waiting for DMA request to clear b0111 = Writing the channel controller data b1000 = Stalled b1001 = Done b1010 = Peripheral scatter-gather transition b1011-b1111 = Undefined	0x0000_0000
MASTER_ENABLE	[0]	R	Enable status of the controller 0 = Controller is disabled 1 = Controller is enabled	0x0000_0000

4.2.4.1.1.2 DMA_CFG

- Base Address: 0x4001_B000
- Address = Base Address + 0x0004, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD0	[31:8]	W	*Reserved	0x0000_0000
CHNL_PROT_CTRL	[7:5]	W	Sets the AHB-Lite protection by controlling the HPROT[3:1] signal levels as follows:	0x0000_0000

Name	Bit	Type	Description	Reset Value
			Bit [7] Controls HPROT[3] to indicate if a cacheable access is occurring. Bit [6] Controls HPROT[2] to indicate if a bufferable access is occurring. Bit [5] Controls HPROT[1] to indicate if a privileged access is occurring. When bit [n] = 1 then the corresponding HPROT is High. When bit [n] = 0 then the corresponding HPROT is Low.	
MASTER_ENABLE	[0]	W	Enable status of the controller 0 = Disables the controller 1 = Enables the controller	0x0000_0000

4.2.4.1.1.3 CTRL_BASE_PTR

- Base Address: 0x4001_B000
- Address = Base Address + 0x0008, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CTRL_BASE_PTR	[31:9]	RW	Pointer to the base address of the primary data structure	0x0000_0000

4.2.4.1.1.4 ALT_CTRL_BASE_PTR

- Base Address: 0x4001_B000
- Address = Base Address + 0x000C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ALT_CTRL_BASE_PTR	[31:0]	R	Base address of the alternate data structure	0x0000_0000

4.2.4.1.1.5 DMA_WAITONREQ_STATUS

- Base Address: 0x4001_B000
- Address = Base Address + 0x0010, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
DMA_WAITONREQ_STATUS	[31:0]	R	Channel wait on request status. Read as: Bit [C] = 0: dma_waitonreq[C] is Low Bit [C] = 1: dma_waitonreq[C] is High	0x0000_0000

4.2.4.1.1.6 CHNL_SW_REQUEST

- Base Address: 0x4001_B000
- Address = Base Address + 0x0014, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CHNL_SW_REQUEST	[31:0]	W	Set the appropriate bit to generate a software DMA request on the corresponding DMA channel. Write as: Bit [C] = 0: Does not create a DMA request for channel C. Bit [C] = 1: Creates a DMA request for channel C. Writing to a bit where a DMA channel is not implemented does not create a DMA request for that channel.	0x0000_0000

4.2.4.1.1.7 CHNL_USEBURST_SET

- Base Address: 0x4001_B000
- Address = Base Address + 0x0018, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CHNL_USEBURST_SET	[31:0]	RW	Returns the useburst status, or disables dma_sreq[C] from generating DMA requests. Read as: Bit [C] = 0: DMA channel C responds to requests that it receives on dma_req[C] or dma_sreq[C]. The controller performs 2R, or single bus transfers. Bit [C] = 1: DMA channel C does not respond to requests that it receives on dma_sreq[C]. The controller only responds to dma_req[C] requests and performs 2R transfers. Write as: Bit [C] = 0: No effect. Use the chnl_useburst_clr register to set bit [C] to 0. Bit [C] = 1: Disables dma_sreq[C] from generating DMA requests. The controller performs 2R transfers. Writing to a bit where a DMA channel is not implemented has no effect.	0x0000_0000

4.2.4.1.1.8 CHNL_USEBURST_CLR

- Base Address: 0x4001_B000
- Address = Base Address + 0x001C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CHNL_USEBURST_CLR	[31:0]	W	Set the appropriate bit to enable dma_sreq[] to generate requests. Write as: Bit [C] = 0: No effect. Use the chnl_useburst_set register to disable dma_sreq[] from generating requests. Bit [C] = 1: Enables dma_sreq[C] to generate DMA requests. Writing to a bit where a DMA channel is not implemented has no effect.	0x0000_0000

4.2.4.1.1.9 CHNL_REQ_MASK_SET

- Base Address: 0x4001_B000
- Address = Base Address + 0x0020, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CHNL_REQ_MASK_SET	[31:0]	RW	Returns the request mask status of dma_req[] and dma_sreq[] or disables the corresponding channel from generating DMA requests. Read as: Bit [C] = 0 External requests are enabled for channel C. Bit [C] = 1 External requests are disabled for channel C. Write as: Bit [C] = 0 No effect. Use the chnl_req_mask_clr register to enable DMA requests. Bit [C] = 1 Disables dma_req[C] and dma_sreq[C] from generating DMA requests. Writing to a bit where a DMA channel is not implemented has no effect.	0x0000_0000

4.2.4.1.1.10 CHNL_REQ_MASK_CLR

- Base Address: 0x4001_B000
- Address = Base Address + 0x0024, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CHNL_REQ_MASK_CLR	[31:0]	W	Set the appropriate bit to enable DMA requests for the channel corresponding to dma_req[] and dma_sreq[]. Write as: Bit [C] = 0 No effect. Use the chnl_req_mask_set register to disable dma_req[] and dma_sreq[] from generating requests. Bit [C] = 1 Enables dma_req[C] or dma_sreq[C] to generate DMA requests. Writing to a bit where a DMA channel is not implemented has no effect.	0x0000_0000

4.2.4.1.1.11 CHNL_ENABLE_SET

- Base Address: 0x4001_B000
- Address = Base Address + 0x0028, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CHNL_ENABLE_SET	[31:0]	RW	Returns the enable status of the channels or enables the corresponding channels. Read as: Bit [C] = 0 Channel C is disabled. Bit [C] = 1 Channel C is enabled.	0x0000_0000

			Write as: Bit [C] = 0 No effect. Use the chnl_enable_clr register to disable a channel. Bit [C] = 1 Enables channel C. Writing to a bit where a DMA channel is not implemented has no effect.	

4.2.4.1.1.12 CHNL_ENABLE_CLR

- Base Address: 0x4001_B000
- Address = Base Address + 0x002C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CHNL_ENABLE_CLR	[31:0]	W	Set the appropriate bit to disable the corresponding DMA channel. Write as: Bit [C] = 0 No effect. Use the chnl_enable_set register to enable DMA channels. Bit [C] = 1 Disables channel C. Writing to a bit where a DMA channel is not implemented has no effect.	0x0000_0000

4.2.4.1.1.13 CHNL_PRI_ALT_SET

- Base Address: 0x4001_B000
- Address = Base Address + 0x0030, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CHNL_PRI_ALT_SET	[31:0]	RW	Returns the channel control data structure status or selects the alternate data structure for the corresponding DMA channel. Read as: Bit [C] = 0 DMA channel C uses the primary data structure. Bit [C] = 1 DMA channel C uses the alternate data structure. Write as: Bit [C] = 0 No effect. Use the chnl_pri_alt_clr register to set bit [C] to 0. Bit [C] = 1 Selects the alternate data structure for channel C. Writing to a bit where a DMA channel is not implemented has no effect.	0x0000_0000

4.2.4.1.1.14 CHNL_PRI_ALT_CLR

- Base Address: 0x4001_B000
- Address = Base Address + 0x0034, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CHNL_PRI_ALT_CLR	[31:0]	W	Set the appropriate bit to select the primary data structure for the corresponding DMA channel. Write as: Bit [C] = 0 No effect. Use the chnl_pri_alt_set register to select the alternate data structure. Bit [C] = 1 Selects the primary data structure for channel C. Writing to a bit where a DMA channel is not implemented has no effect.	0x0000_0000

4.2.4.1.1.15 CHNL_PRIORITY_SET

- Base Address: 0x4001_B000
- Address = Base Address + 0x0038, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CHNL_PRIORITY_SET	[31:0]	RW	Returns the channel priority mask status, or sets the channel priority to high. Read as: Bit [C] = 0: DMA channel C uses the default priority level. Bit [C] = 1: DMA channel C is using a high priority level. Write as: Bit [C] = 0: No effect. Use the chnl_priority_clr Register to set channel C to the default priority level. Bit [C] = 1: Channel C uses the high priority level. Writing to a bit where a DMA channel is not implemented has no effect.	0x0000_0000

4.2.4.1.1.16 CHNL_PRIORITY_CLR

- Base Address: 0x4001_B000
- Address = Base Address + 0x003C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CHNL_PRIORITY_CLR	[31:0]	W	Set the appropriate bit to select the default priority level for the specified DMA channel. Write as: Bit [C] = 0: No effect. Use the chnl_priority_set register to set channel C to the high priority level. Bit [C] = 1: Channel C uses the default priority level. Writing to a bit where a DMA channel is not implemented has no effect.	0x0000_0000

4.2.4.1.1.17 ERR_CLR

- Base Address: 0x4001_B000
- Address = Base Address + 0x004C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD0	[31:1]	RW	*Reserved	0x0000_0000
ERR_CLR	[0]	RW	Returns the status of dma_err or sets the signal to Low. Read as: 0 = dma_err is Low 1 = dma_err is High Write as: 0 = No effect, status of dma_err is unchanged. 1 = Sets dma_err Low. For test purposes, use the err_set register to set dma_err as High.	0x0000_0000

4.2.4.1.1.18 DMA_MUX

- Base Address: 0x4001_B000
- Address = Base Address + 0x0050, Reset Value = 0x3210_3210

Name	Bit	Type	Description	Reset Value
RSVD	[31]	RW	*Reserved	0x00000000
SPI_CH3_MUX	[30:28]	RW	SPI_CH3 DMA mapping selection 3'd0: SPI0 3'd1: SPI1 3'd2: SPI2 3'd3: SPI3 3'd4: SPI4	0x00000003
RSVD	[27]	RW	*Reserved	0x00000000
SPI_CH2_MUX	[26:24]	RW	SPI_CH2 DMA mapping selection 3'd0: SPI0 3'd1: SPI1 3'd2: SPI2 3'd3: SPI3 3'd4: SPI4	0x00000002
RSVD	[23]	RW	*Reserved	0x00000000
SPI_CH1_MUX	[22:20]	RW	SPI_CH1 DMA mapping selection 3'd0: SPI0 3'd1: SPI1 3'd2: SPI2 3'd3: SPI3 3'd4: SPI4	0x00000001

Name	Bit	Type	Description	Reset Value
RSVD	[19]	RW	*Reserved	0x00000000
SPI_CH0_MUX	[18:16]	RW	SPI_CH0 DMA mapping selection 3'd0: SPI0 3'd1: SPI1 3'd2: SPI2 3'd3: SPI3 3'd4: SPI4	0x00000000
RSVD	[15]	RW	*Reserved	0x00000000
I2C_CH3_MUX	[14:12]	RW	I2C_CH3 DMA mapping selection 3'd0: I2C0 3'd1: I2C1 3'd2: I2C2 3'd3: I2C3 3'd4: I2C4	0x00000003
RSVD	[11]	RW	*Reserved	0x00000000
I2C_CH2_MUX	[10:8]	RW	I2C_CH2 DMA mapping selection 3'd0: I2C0 3'd1: I2C1 3'd2: I2C2 3'd3: I2C3 3'd4: I2C4	0x00000002
RSVD	[7]	RW	*Reserved	0x00000000
I2C_CH1_MUX	[6:4]	RW	I2C_CH1 DMA mapping selection 3'd0: I2C0 3'd1: I2C1 3'd2: I2C2 3'd3: I2C3 3'd4: I2C4	0x00000001
RSVD	[3]	RW	*Reserved	0x00000000
I2C_CH0_MUX	[2:0]	RW	I2C_CH0 DMA mapping selection 3'd0: I2C0 3'd1: I2C1 3'd2: I2C2 3'd3: I2C3 3'd4: I2C4	0x00000000

4.2.4.1.1.19 DMA_NOT_MUX

- Base Address: 0x4001_B000
- Address = Base Address + 0x0054, Reset Value = 0x0000_0044

Name	Bit	Type	Description	Reset Value
RSVD	[7]	RW	*Reserved	0x00000000
SPI_NOT_MUX	[6:4]	RW	DMA unmapped SPI selection 3'd0: SPI0 3'd1: SPI1 3'd2: SPI2 3'd3: SPI3 3'd4: SPI4	0x00000004
RSVD	[3]	RW	*Reserved	0x00000000
I2C_NOT_MUX	[2:0]	RW	DMA unmapped I2C selection 3'd0: I2C0 3'd1: I2C1 3'd2: I2C2 3'd3: I2C3 3'd4: I2C4	0x00000004

4.2.4.1.1.20 DMA_REQ_GATE

- Base Address: 0x4001_B000
- Address = Base Address + 0x0058, Reset Value = 0xFFFF_FFFF

Name	Bit	Type	Description	Reset Value
DMA_REQ_GATE	[31:0]	RW	DMA Request gating enable ([0] ~ [31] channel) 1'b1: Enable DMA request (not gating) 1'b0: Disable DMA request (gating)	0xFFFF_FFFF

4.2.4.1.1.21 PERIPH_ID_4

- Base Address: 0x4001_B000
- Address = Base Address + 0x0FD0, Reset Value = 0x0000_0004

Name	Bit	Type	Description	Reset Value
BLOCK_COUNT	[7:4]	R	The number of 4 KB address blocks required to access the registers, expressed in powers of 2. These bits are read back as 0x0.	0x0000_0000
JEP106_C_CODE	[3:0]	R	The JEP106 continuation code value represents the number of 0x7F continuation characters that occur in the identity code of manufacturer. These bits are read back as 0x4.	0x0000_0004

4.2.4.1.1.22 PERIPH_ID_0

- Base Address: 0x4001_B000
- Address = Base Address + 0x0FE0, Reset Value = 0x0000_0030

Name	Bit	Type	Description	Reset Value
PART_NUMBER0	[7:0]	R	These bits are read back as 0x30.	0x0000_0030

4.2.4.1.1.23 PERIPH_ID_1

- Base Address: 0x4001_B000
- Address = Base Address + 0x0FE4, Reset Value = 0x0000_00B2

Name	Bit	Type	Description	Reset Value
JEP106_ID_3_0	[7:4]	R	JEP106 identity code [3:0]. These bits are read back as 0xB because ARM is the designer of the peripheral.	0x0000_000B
PART_NUMBER1	[3:0]	R	These bits are read back as 0x2.	0x0000_0002

4.2.4.1.1.24 PERIPH_ID_2

- Base Address: 0x4001_B000
- Address = Base Address + 0x0FE8, Reset Value = 0x0000_000B

Name	Bit	Type	Description	Reset Value
REVISION	[7:4]	R	The revision status of the controller. For revision r0p0, these bits are read back as 0x0.	0x0000_0000
JEDEC_USED	[3]	R	JEP106 identity code [3:0]. These bits are read back as 0xB because ARM is the designer of the peripheral.	0x0000_0001
JEP106_ID_6_4	[2:0]	R	These bits are read back as 0x2.	0x0000_0003

4.2.4.1.1.25 PERIPH_ID_3

- Base Address: 0x4001_B000
- Address = Base Address + 0x0FEC, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
MOD_NUMBER	[3:0]	R	The customer must update this field if they modify the RTL of the controller. ARM sets this bit to 0x0.	0x0000_0000

4.2.4.1.1.26 PCELL_ID_0

- Base Address: 0x4001_B000
- Address = Base Address + 0x0FF0, Reset Value = 0x0000_000D

Name	Bit	Type	Description	Reset Value
PCELL_ID_0	[7:0]	R	These bits are read back as 0x0D.	0x0000_000D

4.2.4.1.1.27 PCELL_ID_1

- Base Address: 0x4001_B000
- Address = Base Address + 0x0FF4, Reset Value = 0x0000_00F0

Name	Bit	Type	Description	Reset Value
PCELL_ID_1	[7:0]	R	These bits are read back as 0xF0.	0x0000_00F0

4.2.4.1.1.28 PCELL_ID_2

- Base Address: 0x4001_B000
- Address = Base Address + 0x0FF8, Reset Value = 0x0000_0005

Name	Bit	Type	Description	Reset Value
PCELL_ID_2	[7:0]	R	These bits are read back as 0x05.	0x0000_0005

4.2.4.1.1.29 PCELL_ID_3

- Base Address: 0x4001_B000
- Address = Base Address + 0x0FFC, Reset Value = 0x0000_00B1

Name	Bit	Type	Description	Reset Value
PCELL_ID_3	[7:0]	R	These bits are read back as 0xB1.	0x0000_00B1

4.2.5 Sample Rate Converter

Sample Rate Converter (SRC) is a type of hardware accelerator which performs resampling data to align the sampling rates of data streams. It supports decimation and interpolation methods. *Figure 4-3* illustrates the block diagram of SRC.

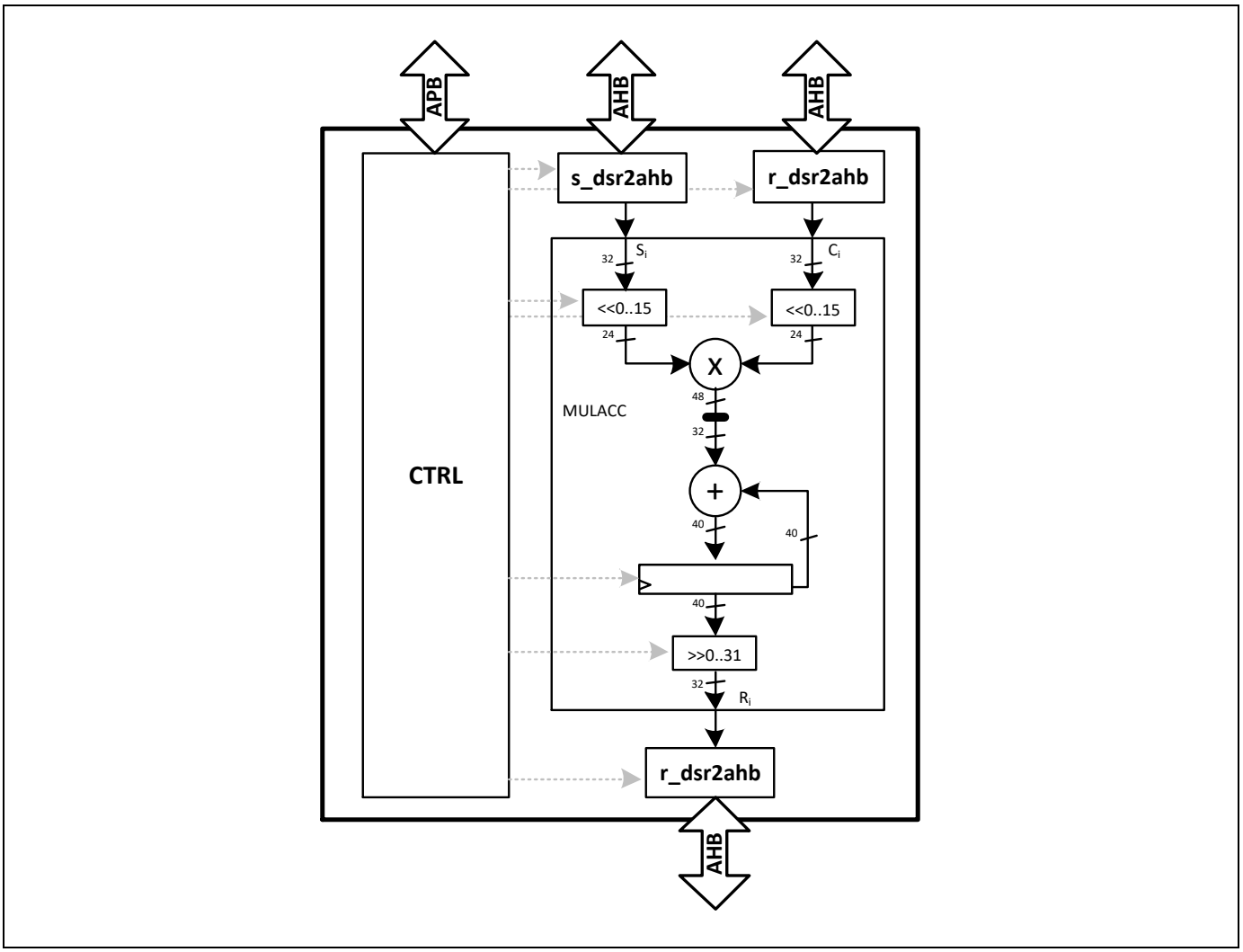


Figure 4-3 Block Diagram of SRC

Following are the two operating methods of rate conversion:

- When resampling is done using (integer) decimation, then you can use a simple algorithm. In that case, the division of the input and output sampling rate is an integer number as illustrated in *Figure 4-4* A.
- When input and output frequency are not an integer multiple of each other, then you must perform the interpolation. The output samples do not directly reuse the input samples and needs to be calculated by means of interpolation as illustrated in *Figure 4-4* B.

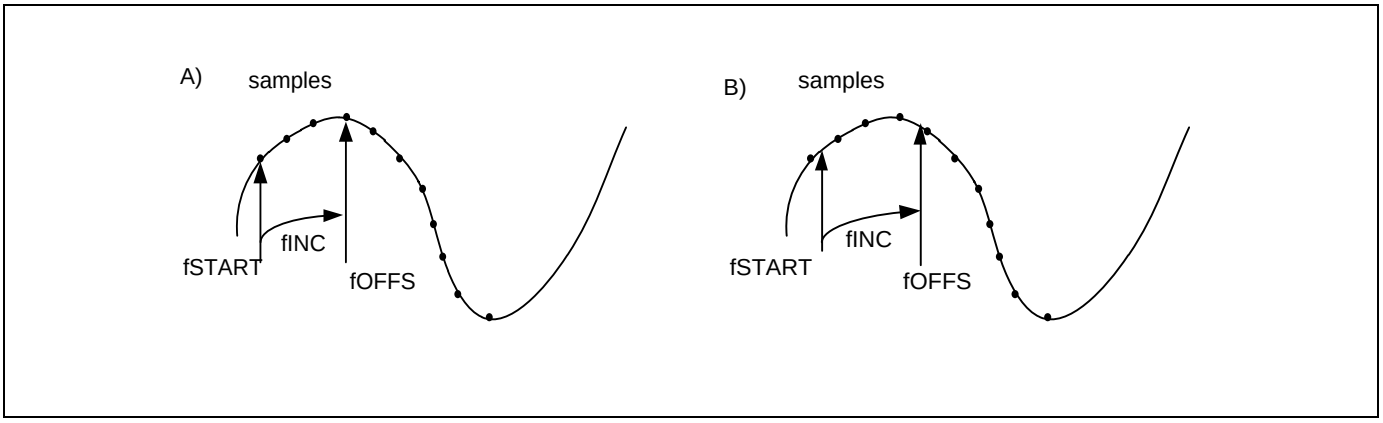


Figure 4-4 Two Operating Methods

4.2.5.1 Detailed Description of the Algorithm

4.2.5.1.1 Algorithm for Decimation-Only SRC

Figure 4-5 illustrates the decimation-only conversion.

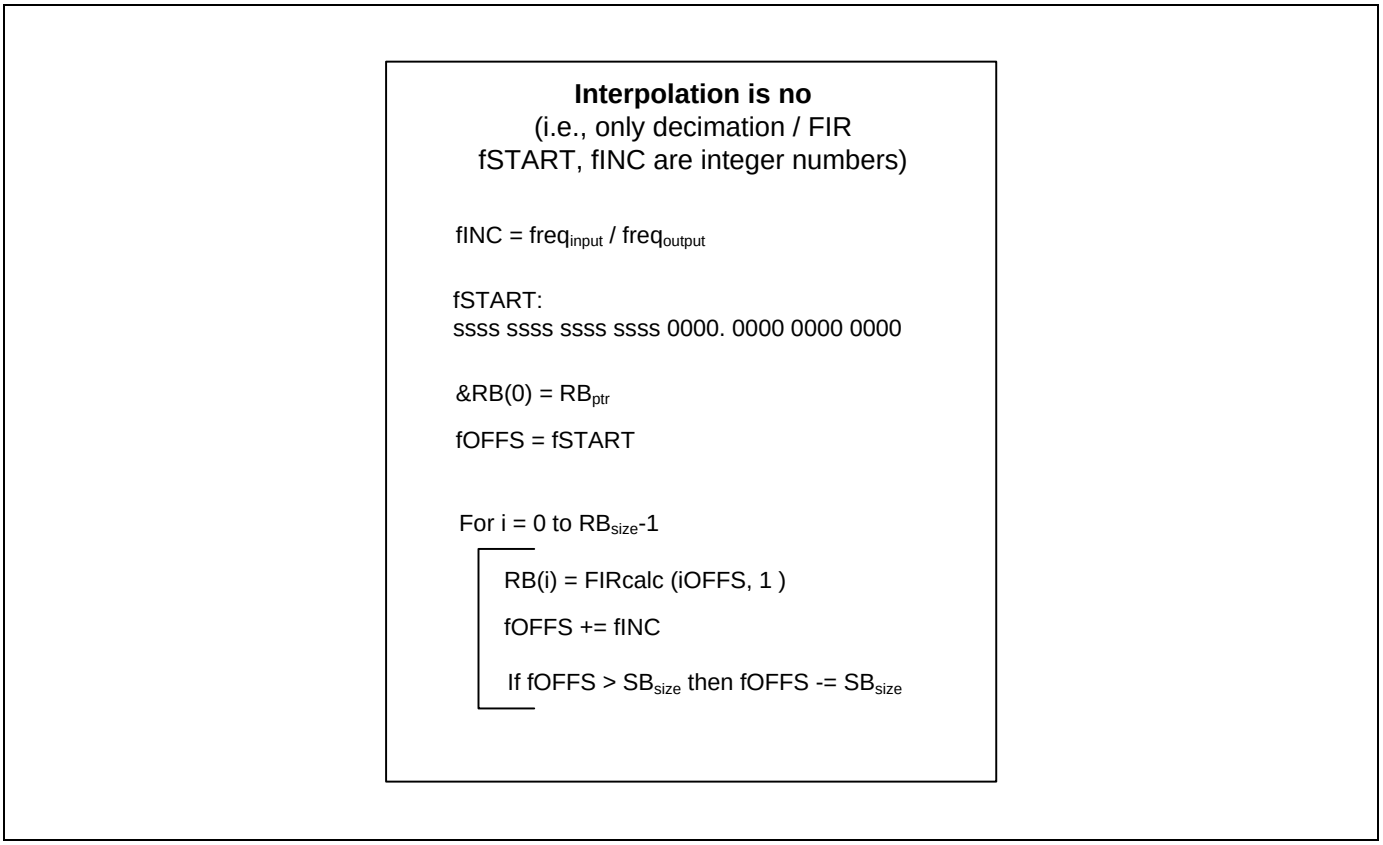


Figure 4-5 Decimation-Only Conversion

4.2.5.1.2 Algorithm for SRC with Interpolation

Figure 4-6 illustrates the conversion with interpolation.

Interpolation is yes
(16 times upsampling will be performed
fSTART, fINC is a float)

$fINC = 16 * freq_{input} / freq_{output}$

fSTART: ssss ssss ssss ssss pppp.ffff ffff ffff
fINC : ssss ssss pppp.ffff ffff ffff ffff ffff
fOFFS : ssss ssss ssss ssss pppp.ffff ffff ffff ffff ffff

$\&RB(0) = RB_{ptr}$

fOFFS = fSTART

For i = 0 to RB_{size}-1

iOFFS = round(fOFFS) == floor (fOFFS + 0.5)

Rx = FIRcalc((iOFFS) ? iOFFS-1 :Sbsize , 16)
Ry = FIRcalc(iOFFS , 16)
Rz = FIRcalc((iOFFS ==SB_{size}) ? 0 : iOFFS+1 , 16)

A = ((Rz + Rx) / 2) – Ry
B = (Rz – Rx) / 2
C = Ry
X = fraction(fOFFS-iOFFS) (20 bits)

RB(i) = (A * X + B) * X + C
fOFFS += fINC
If fOFFS > SB_{size} then fOFFS -= SB_{size}

Figure 4-6 Conversion with Interpolation

4.2.5.2 Register Description

This section describes the register map information and its associated registers.

4.2.5.2.1 Register Map Summary

- Base Address: 0x4001_D000

Register	Offset	Description	Reset Value
CTRL	0x0000	CTRL	0x0000_0000
CFG	0x0004	CFG	0x0000_0000
STAT	0x0008	STAT	0x0000_0000
fSTART	0x000C	fSTART	0x0000_0000
fINC	0x0010	fINC	0x0000_0000
PB_PTR	0x0014	PB_PTR	0x0000_0000
PB_SIZE	0x0018	PB_SIZE	0x0000_0000
SB_PTR	0x001C	SB_PTR	0x0000_0000
SB_SIZE	0x0020	SB_SIZE	0x0000_0000
CB_PTR	0x0024	CB_PTR	0x0000_0000
CB_SIZE	0x0028	CB_SIZE	0x0000_0000
RB_PTR	0x002C	RB_PTR	0x0000_0000
RB_SIZE	0x0030	RB_SIZE	0x0000_0000
IN_SH	0x0034	IN_SH	0x0000_0000
OUT_SH	0x0038	OUT_SH	0x0000_0206
INTERRUPT	0x003C	Interrupt	0x0000_0000

NOTE: If reserved or empty addresses in the register map are changed, S1SBP6A cannot guarantee normal operation.

4.2.5.2.1.1 CTRL

- Base Address: 0x4001_D000
- Address = Base Address + 0x0000, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CTRL	[8]	W	Resets the internal state of the sample rate convertor to abort the current operation. It is automatically cleared.	0x0
START	[0]	W	Starts the sample rate convertor. It is automatically cleared.	0x0

4.2.5.2.1.2 CFG

- Base Address: 0x4001_D000
- Address = Base Address + 0x0004, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSIZE	[3]	RW	Selects the access size of result buffer 0 = Valid 24-bit in word access 1 = Valid 16-bit in word access	0x0
SSIZE	[2]	RW	Selects the access sizes of preceding sample buffer and sample buffer 0 = Valid 24-bit in word access 1 = Valid 16-bit in word access	0x0
CSIZE	[1]	RW	Selects the access sizes of coefficient buffer 0 = Valid 24-bit in word access 1 = Valid 16-bit in word access	0x0
Interpolation	[0]	RW	Enables the interpolation mode 0 = Disable interpolation 1 = Enable interpolation	0x0

4.2.5.2.1.3 STAT

- Base Address: 0x4001_D000
- Address = Base Address + 0x0008, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
FIRREADY	[1]	R	FIRCalc state machine ready	0x0
READY	[0]	R	Sample rate converter module ready	0x0

4.2.5.2.1.4 fSTART

- Base Address: 0x4001_D000
- Address = Base Address + 0x000C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
SAMPLE	[31:20]	RW	Sample part of fSTART	0x000
PHASE	[19:16]	RW	Phase part of fSTART	0x0
FRACTION	[15:0]	RW	Fractional part of fSTART	0x0000

4.2.5.2.1.5 fINC

- Base Address: 0x4001_D000
- Address = Base Address + 0x0010, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
SAMPLE	[31:24]	RW	Sample part of fINC	0x000
PHASE	[23:20]	RW	Phase part of fINC	0x0
FRACTION	[19:0]	RW	Fractional part of fINC	0x0000

4.2.5.2.1.6 PB_PTR

- Base Address: 0x4001_D000
- Address = Base Address + 0x0014, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
PB_PTR	[23:0]	RW	Preceding buffer pointer	0x00_0000

4.2.5.2.1.7 PB_SIZE

- Base Address: 0x4001_D000
- Address = Base Address + 0x0018, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
PB_SIZE	[15:0]	RW	Preceding buffer size	0x0000

4.2.5.2.1.8 SB_PTR

- Base Address: 0x4001_D000
- Address = Base Address + 0x001c, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
SB_asel	[31]	RW	Selects the target SRAM of sample buffer 0 = SRAM in MCU 1 = SRAM in SRP	0x0
SB_PTR	[23:0]	RW	Sample buffer pointer	0x00_0000

4.2.5.2.1.9 SB_SIZE

- Base Address: 0x4001_D000
- Address = Base Address + 0x0020, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
SB_SIZE	[15:0]	RW	Sample buffer size	0x0000

4.2.5.2.1.10 CB_PTR

- Base Address: 0x4001_D000
- Address = Base Address + 0x0024, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CB_asel	[31]	RW	Selects the target SRAM of coefficient buffer 0 = SRAM in MCU 1 = SRAM in SRP	0x0
CB_PTR	[23:0]	RW	Coefficient buffer pointer	0x00_0000

4.2.5.2.1.11 CB_SIZE

- Base Address: 0x4001_D000
- Address = Base Address + 0x0028, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CB_SIZE	[15:0]	RW	Coefficient buffer size	0x0000

4.2.5.2.1.12 RB_PTR

- Base Address: 0x4001_D000
- Address = Base Address + 0x002c, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RB_asel	[31]	RW	Selects the target SRAM of result buffer 0 = SRAM in MCU 1 = SRAM in SRP	0x0
RB_PTR	[23:0]	RW	Result buffer pointer	0x00_0000

4.2.5.2.1.13 RB_SIZE

- Base Address: 0x4001_D000
- Address = Base Address + 0x0030, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RB_SIZE	[15:0]	RW	Result buffer size	0x0000

4.2.5.2.1.14 IN_SH

- Base Address: 0x4001_D000
- Address = Base Address + 0x0034, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CB_SH	[11:8]	RW	Left shift the 16/24-bits word of Coeff. Buffer into position for the next stage	0x0
SB_SH	[3:0]	RW	Left shift the 16/24-bits word of sample buffer into position for the next stage	0x0

4.2.5.2.1.15 OUT_SH

- Base Address: 0x4001_D000
- Address = Base Address + 0x0038, Reset Value = 0x0000_0206

Name	Bit	Type	Description	Reset Value
OR_SH	[12:8]	RW	Right shift the result into position for output to the memory	0x2
MA_SH	[3:0]	RW	Right shift the 40 bits output of the MACC for further processing	0x6

4.2.5.2.1.16 INTERRIPT

- Base Address: 0x4001_D000
- Address = Base Address + 0x003C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
INT_MASK	[1]	RW	Interrupt mask	0x0
INT_CLEAR	[0]	RW	Interrupt clear	0x0

4.2.6 General Purpose I/O

GPIO is a General Purpose I/O interface unit. It provides a 16 bits I/O interface for each GPIO port with the following properties:

- Programmable interrupt generation capability
- Bit masking support using address values
- Registers for alternate function switching with pin multiplexing
- Thread safe operation by providing separate set and clear addresses for control registers
- Inputs are sampled using a double flip-flop to avoid meta-stability issues.

Figure 4-7 illustrates the control circuit and external interface of the GPIO.

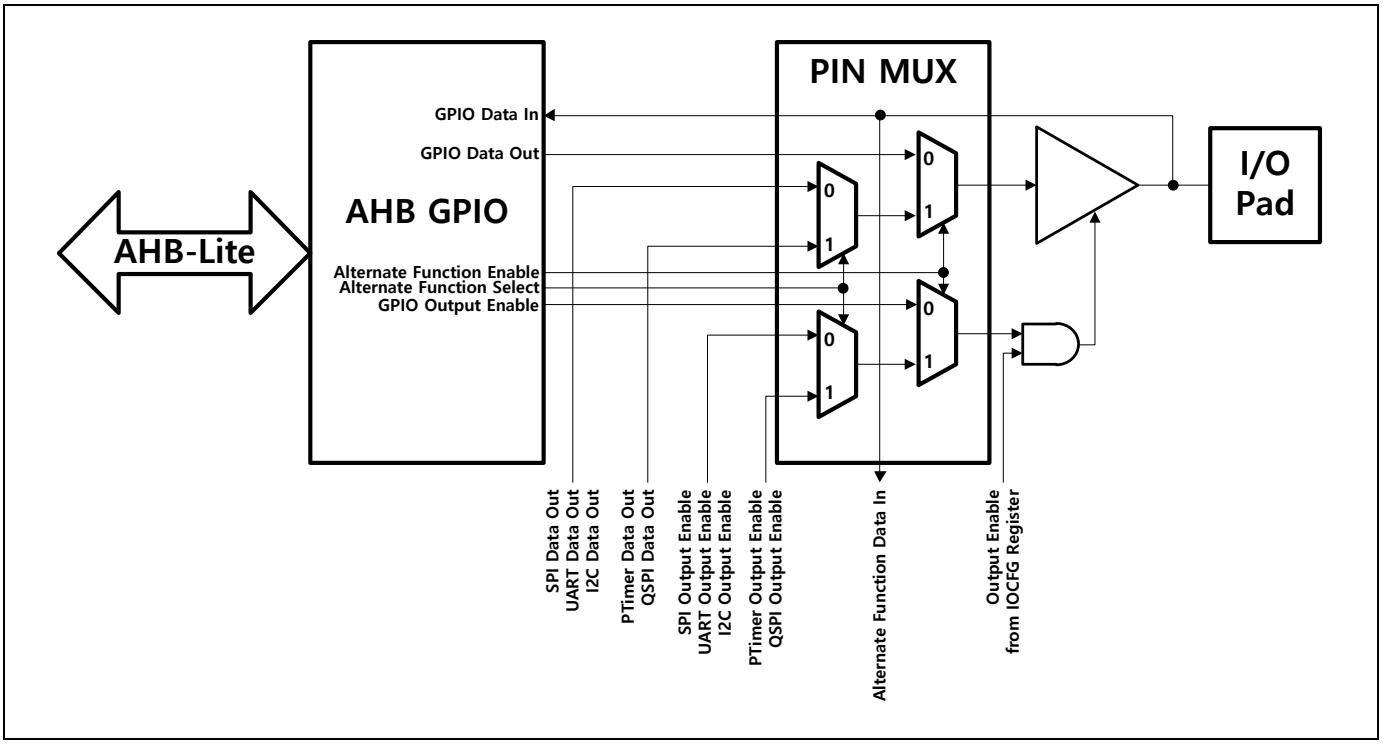


Figure 4-7 GPIO Control Circuit and External Interface

4.2.6.1 Interrupt Generation

The AHB GPIO provides programmable interrupt generation features. Three registers such as Interrupt enable[n], Interrupt polarity[n] and Interrupt type[n] control this and each register has separate set and clear addresses. You can configure each bit of the I/O pins to generate interrupts based on these registers.

After an interrupt is triggered, the corresponding bit in the INTSTATUS register is set. This also causes the corresponding bit of the GPIOINT[15:0] signal to be asserted. As a result, the combined interrupt signal, COMBINT, is also asserted. You can clear the interrupt status using an interrupt handler that writes 1 to the corresponding bit of the INTCLEAR register, that is, the same address as the INTSTATUS Register.

4.2.6.2 Masked Access

The masked access feature permits individual bits or multiple bits, to be read from or written to in a single transfer. This avoids software-based read-modify-write operations that are not thread safe. With the masked access operations, the 16 bits I/O is divided into two halves, lower byte, and the upper byte. The bit mask address spaces are defined as two arrays, each containing 256 words.

For example, if you must set bits[1:0] both to 1, and clear bits [7:6] in a single operation, you can use the lower byte mask access address space to perform this write operation. The required bit mask is 0xC3, and you can write the operation as MASKLOWBYTE[0xC3] = 0x03 as illustrated in *Figure 4-8*.

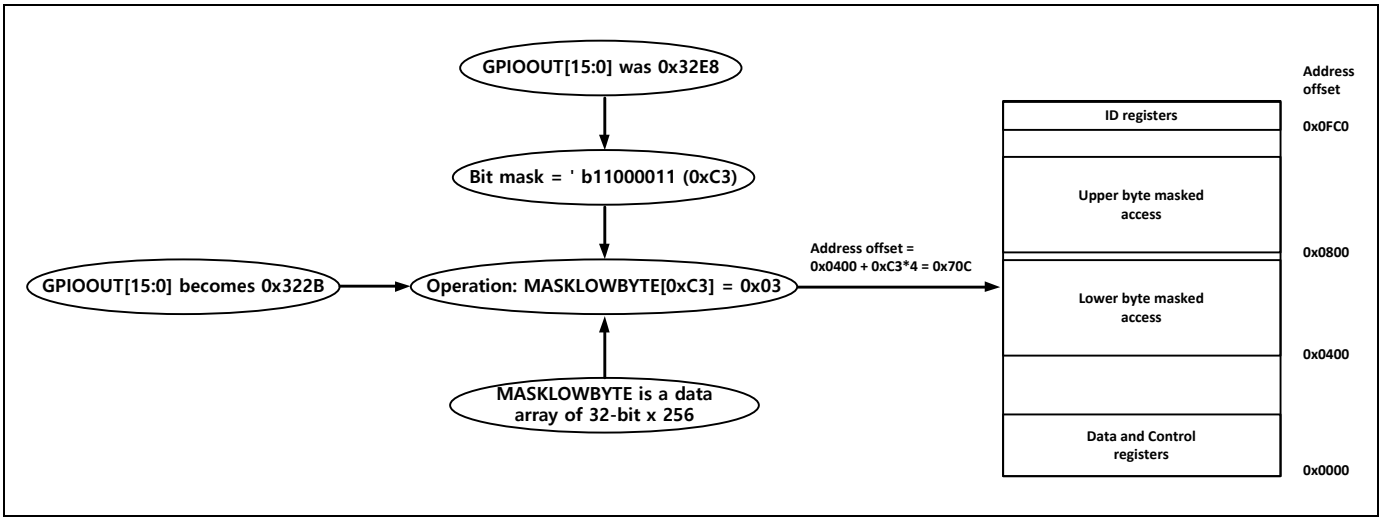


Figure 4-8 Masked Access 1

Similarly, if you must update some of the bits in the upper eight bits of the GPIO port, you must use the MASKHIGHBYTE array as illustrated in *Figure 4-9*.

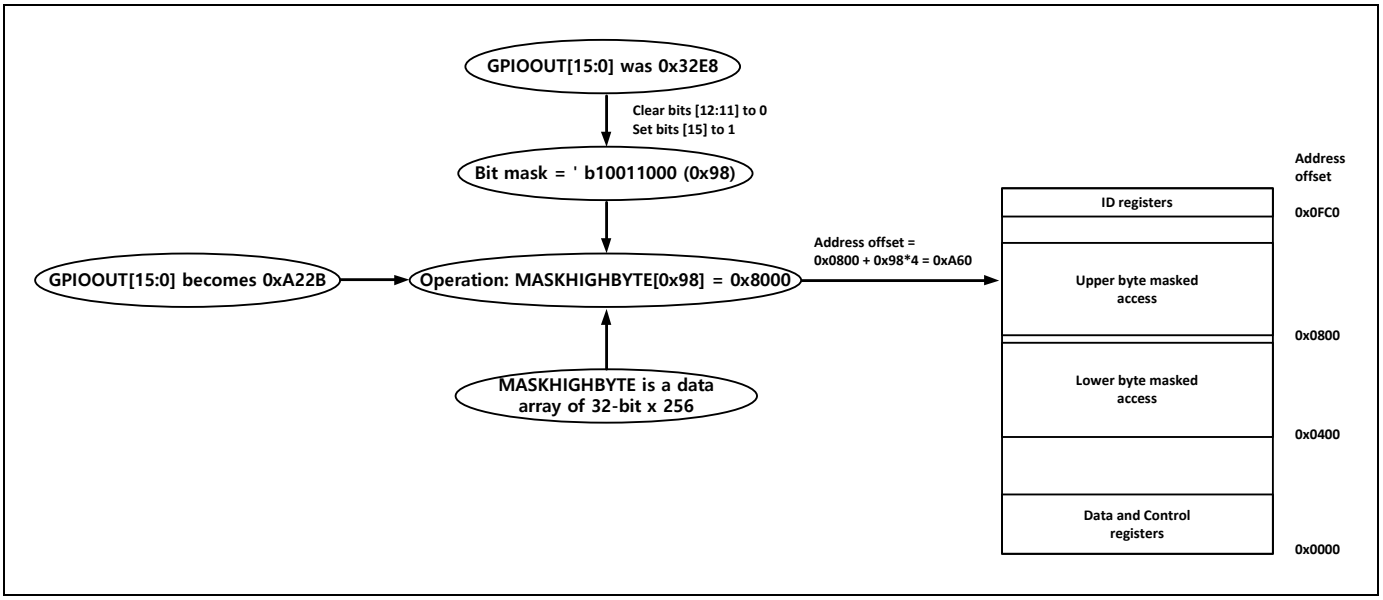


Figure 4-9 Masked Access 2

4.2.6.3 Register Description

This section describes the register map information and its associated registers.

4.2.6.3.1 Register Map Summary

- Base Address: 0x4002_0000

Register	Offset	Description	Reset Value
DATA	0x0000	*Data value Read Sampled at pin Write To data output register Read back value goes through double flip-flop synchronization logic with a delay of two cycles	0x0000_0000
DATAOUT	0x0004	*Data output register value Read Current value of data output register Write To data output register	0x0000_0000
OUTENSET	0x0010	*Output enable set Write 0 = No effect 1 = Set the output enable bit Read 0 = Indicate the signal direction as input 1 = Indicate the signal direction as output	0x0000_0000
OUTENCLR	0x0014	*Output enable clear Write 0 = No effect 1 = Clear the output enable bit Read 0 = Indicate the signal direction as input 1 = Indicate the signal direction as output	0x0000_0000
ALTFUNCSET	0x0018	*Alternative function set Write 0 = No effect 1 = Set the ALTFUNC bit Read 0 = For I/O 1 = For an alternate function	0x0000_0000
ALTFUNCCLR	0x001C	*Alternative function clear Write 0 = No effect 1 = Clear the ALTFUNC bit Read 0 = For I/O 1 = For an alternate function	0x0000_0000

Register	Offset	Description	Reset Value
INTENSET	0x0020	*Interrupt enable set Write 0 = No effect 1 = Set the enable bit Read 0 = Interrupt disabled 1 = Interrupt enabled	0x0000_0000
INTENCLR	0x0024	*Interrupt enable clear Write 0 = No effect 1 = Clear the enable bit Read 0 = Interrupt disabled 1 = Interrupt enable	0x0000_0000
INTTYPESET	0x0028	*Interrupt type set Write 0 = No effect 1 = Set the interrupt type bit Read 0 = For Low or High level 1 = For falling edge or rising edge	0x0000_0000
INTTYPECLR	0x002C	*Interrupt type clear Write 0 = No effect 1 = Clear the interrupt type bit Read 0 = For Low or High level 1 = For falling edge or rising edge	0x0000_0000
INTPOLSET	0x0030	*Polarity-level and edge IRQ configuration Write 0 = No effect 1 = Set the interrupt polarity bit Read 0 = For Low level or falling edge 1 = For High level or rising edge	0x0000_0000
INTPOLCLR	0x0034	*Polarity-level and edge IRQ configuration Write 0 = No effect 1 = Clear the interrupt polarity bit Read 0 = For Low level or falling edge 1 = For High level or rising edge	0x0000_0000

Register	Offset	Description	Reset Value
INTSTATUS_INTCLEAR	0x0038	*Write 1 to clear interrupt request Write [15:0] IRQ status clear register 0 = No effect 1 = To clear the interrupt request Read [15:0] IRQ status Register	0x0000_0000
ALTFUNCSEL	0x003C	*Alternative function selection Write bit to select one of two alternative functions	0x0000_0000
MASKLOWBYTE#	0x0400 ~ 0x07FF	*Lower eight bits masked access. Bits [9:2] of the address value are used as enable bit mask for the access [15:8] Not used. Write is ignored and read as 0. [7:0] Data for lower byte access with [9:2] of address value used as enable mask for each bit.	0x0000_0000
MASKHIGHBYTE#	0x0800 ~ 0x0BFF	*Higher eight bits masked access. Bits [9:2] of the address value are used as enable bit mask for the access [15:8] Data for higher byte access with [9:2] of address value used as enable mask for each bit [7:0] Not used. Write is ignored and read as 0.	0x0000_0000
PID4	0x0FD0	*Peripheral ID Register 4 [7:4] Block count [3:0] jep106_c_code	0x0000_0004
PID5	0x0FD4	Peripheral ID Register 5	0x0000_0000
PID6	0x0FD8	Peripheral ID Register 6	0x0000_0000
PID7	0x0FDC	Peripheral ID Register 7	0x0000_0000
PID0	0x0FE0	*Peripheral ID Register 0 [7:0] Part number[7:0]	0x0000_0020
PID1	0x0FE4	*Peripheral ID Register 1 [7:4] jep106_id_3_0 [3:0] Part number[11:8]	0x0000_00B8
PID2	0x0FE8	*Peripheral ID Register 2 [7:4] Revision [3] jedec_used [2:0] jep106_id_6_4	0x0000_000B
PID3	0x0FEC	*Peripheral ID Register 3 [7:4] ECO revision number [3:0] Customer modification number	0x0000_0000
CID0	0x0FF0	Component ID Register 0	0x0000_000D
CID1	0x0FF4	Component ID Register 1	0x0000_00F0
CID2	0x0FF8	Component ID Register 2	0x0000_0005
CID3	0x0FFC	Component ID Register 3	0x0000_00B1

NOTE: If reserved or empty addresses in the register map are changed, S1SBP6A cannot guarantee normal operation.

4.2.6.3.1.1 DATA

- Base Address: 0x4002_0000
- Address = Base Address + 0x0000, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
DATA	[15:0]	RW	*Data value Read Sampled at pin Write To data output register Read back value goes through double flip-flop synchronization logic with a delay of two cycles.	0x0000_0000

4.2.6.3.1.2 DATAOUT

- Base Address: 0x4002_0000
- Address = Base Address + 0x0004, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
DATAOUT	[15:0]	RW	*Data output Register value Read Current value of data output register Write To data output register	0x0000_0000

4.2.6.3.1.3 OUTENSET

- Base Address: 0x4002_0000
- Address = Base Address + 0x0010, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
OUTENSET	[15:0]	RW	*Output enable set Write 0 = No effect 1 = Set the output enable bit Read 0 = Indicate the signal direction as input 1 = Indicate the signal direction as output	0x0000_0000

4.2.6.3.1.4 OUTENCLR

- Base Address: 0x4002_0000
- Address = Base Address + 0x0014, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
OUTENCLR	[15:0]	RW	*Output enable clear Write 0 = No effect 1 = Clear the output enable bit Read 0 = Indicate the signal direction as input 1 = Indicate the signal direction as output	0x0000_0000

4.2.6.3.1.5 ALTFUNCSET

- Base Address: 0x4002_0000
- Address = Base Address + 0x0018, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ALTFUNCSET	[15:0]	RW	*Alternative function set Write 0 = No effect 1 = Set the ALTFUNC bit Read 0 = For I/O 1 = For an alternate function	0x0000_0000

4.2.6.3.1.6 ALTFUNCCLR

- Base Address: 0x4002_0000
- Address = Base Address + 0x001C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ALTFUNCCLR	[15:0]	RW	*Alternative function clear Write 0 = No effect 1 = Clear the ALTFUNC bit Read 0 = For I/O 1 = For an alternate function	0x0000_0000

4.2.6.3.1.7 INTENSET

- Base Address: 0x4002_0000
- Address = Base Address + 0x0020, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
INTENSET	[15:0]	RW	*Interrupt enable set Write 0 = No effect 1 = Set the enable bit Read 0 = Interrupt disabled 1 = Interrupt enabled	0x0000_0000

4.2.6.3.1.8 INTENCLR

- Base Address: 0x4002_0000
- Address = Base Address + 0x0024, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
INTENCLR	[15 =0]	RW	*Interrupt enable clear Write 0 = No effect 1 = Clear the enable bit Read 0 = Interrupt disabled 1 = Interrupt enable	0x0000_0000

4.2.6.3.1.9 INTTYPESET

- Base Address: 0x4002_0000
- Address = Base Address + 0x0028, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
INTTYPESET	[15:0]	RW	*Interrupt type set Write 0 = No effect 1 = Set the interrupt type bit Read 0 = For Low or High level 1 = For falling edge or rising edge	0x0000_0000

4.2.6.3.1.10 INTTYPECLR

- Base Address: 0x4002_0000
- Address = Base Address + 0x002C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
INTTYPECLR	[15:0]	RW	*Interrupt type clear Write 0 = No effect 1 = Clear the interrupt type bit Read 0 = For Low or High level 1 = For falling edge or rising edge	0x0000_0000

4.2.6.3.1.11 INTPOLSET

- Base Address: 0x4002_0000
- Address = Base Address + 0x0030, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
INTPOLSET	[15:0]	RW	*Polarity-level and edge IRQ configuration Write 0 = No effect 1 = Set the interrupt polarity bit Read 0 = For Low level or falling edge 1 = For High level or rising edge	0x0000_0000

4.2.6.3.1.12 INTPOLCLR

- Base Address: 0x4002_0000
- Address = Base Address + 0x0034, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
INTPOLCLR	[15:0]	RW	*Polarity-level and edge IRQ configuration Write 0 = No effect 1 = Clear the interrupt polarity bit Read 0 = For Low level or falling edge 1 = For High level or rising edge	0x0000_0000

4.2.6.3.1.13 INTSTATUS_INTCLEAR

- Base Address: 0x4002_0000
- Address = Base Address + 0x0038, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
INTSTATUS_INTCLEAR	[15:0]	RW	*Write 1 to clear interrupt request Write [15:0] IRQ status clear register 0 = No effect 1 = To clear the interrupt request Read [15:0] IRQ status register	0x0000_0000

4.2.6.3.1.14 ALTFUNCSEL

- Base Address: 0x4002_0000
- Address = Base Address + 0x003C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
AFSEL_F	[15]	RW	*Alternative function selection for GPIO0F 0 = SPI4 1 = Timer 4 external input *Alternative function selection for GPIO1F 0 = I2C4 1 = No effect *Alternative function selection for GPIO2F 0 = No effect 1 = QSPI	0x0000_0000
AFSEL_E	[14]	RW	*Alternative function selection for GPIO0E 0 = SPI4 1 = Timer 3 external input *Alternative function selection for GPIO1E 0 = I2C4 1 = No effect *Alternative function selection for GPIO2E 0 = No effect 1 = QSPI	0x0000_0000
AFSEL_D	[13]	RW	*Alternative function selection for GPIO0D 0 = SPI4 1 = Timer 2 external input *Alternative function selection for GPIO1D 0 = I2C3 1 = No effect *Alternative function selection for GPIO2D 0 = No effect 1 = QSPI	0x0000_0000

Name	Bit	Type	Description	Reset Value
AFSEL_C	[12]	RW	*Alternative function selection for GPIO0C 0 = SPI4 1 = Timer 1 external input *Alternative function selection for GPIO1C 0 = I2C3 1 = No effect *Alternative function selection for GPIO2C = 0 = No effect 1 = QSPI	0x0000_0000
AFSEL_B	[11]	RW	*Alternative function selection for GPIO0B 0 = SPI3 1 = No effect *Alternative function selection for GPIO1B 0 = I2C2 1 = No effect *Alternative function selection for GPIO2B 0 = No effect 1 = QSPI	0x0000_0000
AFSEL_A	[10]	RW	*Alternative function selection for GPIO0A 0 = SPI3 1 = No effect *Alternative function selection for GPIO1A 0 = I2C2 1 = No effect *Alternative function selection for GPIO2A 0 = Timer 0 external input 1 = QSPI	0x0000_0000
AFSEL_9	[9]	RW	*Alternative function selection for GPIO09 0 = SPI3 1 = No effect *Alternative function selection for GPIO19 0 = I2C1 1 = No effect *Alternative function selection for GPIO29 0 = I2C0 1 = No effect	0x0000_0000
AFSEL_8	[8]	RW	*Alternative function selection for GPIO08 0 = SPI3 1 = No effect *Alternative function selection for GPIO18 0 = I2C1 1 = No effect *Alternative function selection for GPIO28	0x0000_0000

Name	Bit	Type	Description	Reset Value
			0 = I2C0 1 = No effect	
AFSEL_7	[7]	RW	*Alternative function selection for GPIO07 0 = SPI2 1 = No effect *Alternative function selection for GPIO17 0 = UART2 1 = PWM Timer 0 external output *Alternative function selection for GPIO27 0 = UART0 1 = No effect	0x0000_0000
AFSEL_6	[6]	RW	*Alternative function selection for GPIO06 0 = SPI2 1 = No effect *Alternative function selection for GPIO16 0 = UART2 1 = 32.768kHz clock output *Alternative function selection for GPIO26 0 = UART0 1 = No effect	0x0000_0000
AFSEL_5	[5]	RW	*Alternative function selection for GPIO05 0 = SPI2 1 = No effect *Alternative function selection for GPIO15 0 = UART2 1 = No effect *Alternative function selection for GPIO25 0 = UART0 1 = No effect	0x0000_0000
AFSEL_4	[4]	RW	*Alternative function selection for GPIO04 0 = SPI2 1 = No effect *Alternative function selection for GPIO14 0 = UART2 1 = No effect *Alternative function selection for GPIO24 0 = UART0 1 = No effect	0x0000_0000
AFSEL_3	[3]	RW	*Alternative function selection for GPIO03 0 = SPI1 1 = No effect *Alternative function selection for GPIO13 0 = UART1	0x0000_0000

Name	Bit	Type	Description	Reset Value
			1 = PWM Timer 0 external input *Alternative function selection for GPIO23 0 = SPI0 1 = No effect	
AFSEL_2	[2]	RW	*Alternative function selection for GPIO02 0 = SPI1 1 = No effect *Alternative function selection for GPIO12 0 = UART1 1 = Timer 6 external input *Alternative function selection for GPIO22 0 = SPI0 1 = No effect	0x0000_0000
AFSEL_1	[1]	RW	*Alternative function selection for GPIO01 0 = SPI1 1 = No effect *Alternative function selection for GPIO11 0 = UART1 1 = No effect *Alternative function selection for GPIO21 0 = SPI0 1 = No effect	0x0000_0000
AFSEL_0	[0]	RW	*Alternative function selection for GPIO00 0 = SPI1 1 = No effect *Alternative function selection for GPIO10 0 = UART1 1 =Timer 5 external input *Alternative function selection for GPIO20 0 = SPI0 1 = No effect	0x0000_0000

4.2.6.3.1.15 MASKLOWBYTE#

- Base Address: 0x4002_0000
- Address = Base Address + 0x0400~0x07FF, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
MASKLOWBYTE	[15:0]	RW	*Lower eight bits masked access. Bits [9:2] of the address value are used as enable bit mask for the access [15:8] Not used. Write is ignored and read as 0 [7:0] Data for lower byte access with [9:2] of address value used as enable mask for each bit	0x0000_0000

4.2.6.3.1.16 MASKHIGHBYTE#

- Base Address: 0x4002_0000
- Address = Base Address + 0x0800~0x0BFF, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
MASKHIGHBYTE	[15:0]	RW	*Higher eight bits masked access. Bits [9:2] of the address value are used as enable bit mask for the access [15:8] Data for higher byte access with [9:2] of address value used as enable mask for each bit [7:0] Not used. Write is ignored and read as 0	0x0000_0000

4.2.6.3.1.17 PID4

- Base Address: 0x4002_0000
- Address = Base Address + 0x0FD0, Reset Value = 0x0000_0004

Name	Bit	Type	Description	Reset Value
PID4	[7:0]	R	*Peripheral ID Register 4 [7:4] Block count [3:0] jep106_c_code	0x0000_0004

4.2.6.3.1.18 PID5

- Base Address: 0x4002_0000
- Address = Base Address + 0x0FD4, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
PID5	[7:0]	R	Peripheral ID Register 5	0x0000_0000

4.2.6.3.1.19 PID6

- Base Address: 0x4002_0000
- Address = Base Address + 0x0FD8, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
PID6	[7:0]	R	Peripheral ID Register 6	0x0000_0000

4.2.6.3.1.20 PID7

- Base Address: 0x4002_0000
- Address = Base Address + 0x0FDC, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
PID7	[7:0]	R	Peripheral ID Register 7	0x0000_0000

4.2.6.3.1.21 PID0

- Base Address: 0x4002_0000
- Address = Base Address + 0x0FE0, Reset Value = 0x0000_0020

Name	Bit	Type	Description	Reset Value
PID0	[7:0]	R	*Peripheral ID Register 0 [7:0] Part number[7:0]	0x0000_0020

4.2.6.3.1.22 PID1

- Base Address: 0x4002_0000
- Address = Base Address + 0x0FE4, Reset Value = 0x0000_00B8

Name	Bit	Type	Description	Reset Value
PID1	[7:0]	R	*Peripheral ID Register 1 [7:4] jep106_id_3_0 [3:0] Part number[11:8]	0x0000_00B8

4.2.6.3.1.23 PID2

- Base Address: 0x4002_0000
- Address = Base Address + 0x0FE8, Reset Value = 0x0000_000B

Name	Bit	Type	Description	Reset Value
PID2	[7:0]	R	*Peripheral ID Register 2 [7:4] Revision [3] jedec_used [2:0] jep106_id_6_4	0x0000_000B

4.2.6.3.1.24 PID3

- Base Address: 0x4002_0000
- Address = Base Address + 0x0FEC, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
PID3	[7:0]	R	*Peripheral ID Register 3 [7 = 4] ECO revision number [3 = 0] Customer modification number	0x0000_0000

4.2.6.3.1.25 CID0

- Base Address: 0x4002_0000
- Address = Base Address + 0x0FF0, Reset Value = 0x0000_000D

Name	Bit	Type	Description	Reset Value
CID0	[7:0]	R	Component ID Register 0	0x0000_000D

4.2.6.3.1.26 CID1

- Base Address: 0x4002_0000
- Address = Base Address + 0x0FF4, Reset Value = 0x0000_00F0

Name	Bit	Type	Description	Reset Value
CID1	[7:0]	R	Component ID Register 1	0x0000_00F0

4.2.6.3.1.27 CID2

- Base Address: 0x4002_0000
- Address = Base Address + 0x0FF8, Reset Value = 0x0000_0005

Name	Bit	Type	Description	Reset Value
CID2	[7:0]	R	Component ID Register 2	0x0000_0005

4.2.6.3.1.28 CID3

- Base Address: 0x4002_0000
- Address = Base Address + 0x0FFC, Reset Value = 0x0000_00B1

Name	Bit	Type	Description	Reset Value
CID3	[7:0]	R	Component ID Register 3	0x0000_00B1

4.2.7 Timers

4.2.7.1 General Purpose Timer

S1SBP6A utilizes timer of CMSDK (ARM DDI 0479B r0p0).

General purpose timer is a 32 bits down-counter with the following features:

- The interrupt request signal is generated when the counter reaches 0. The interrupt request is held until it is cleared by writing to the INTCLEAR register.
- If the timer count reaches 0 and the software clears a previous interrupt status at the same time, then the interrupt status is set to 1.
- Timer can be enabled when the 0 to 1 transition of external input signal occurs.
- External clock must be half as slow as the peripheral clock, because it is sampled by a double flip-flop and then goes through edge-detection logic when the external inputs act as a clock.

4.2.7.1.1 Register Description

This section describes the register map information and its associated registers.

4.2.7.1.1.1 Register Map Summary

- Base Address: 0x4000_0000

Register	Offset	Description	Reset Value
CTRL	0x0000	[3] Timer interrupt enable [2] Select external input as clock [1] Select external input as enable [0] Enable	0x0000_0000
VALUE	0x0004	Current value	0x0000_0000
RELOAD	0x0008	Reload value. A write to this register sets the current value	0x0000_0000
INTERRUPT	0x000C	Write: Timer interrupt. Write 1 to clear this field. Read: Timer interrupt status	0x0000_0000
PID4	0x0FD0	*Peripheral ID Register 4 [7:4] Block count [3:0] jep106_c_code	0x0000_0004
PID5	0x0FD4	Peripheral ID Register 5	0x0000_0000
PID6	0x0FD8	Peripheral ID Register 6	0x0000_0000
PID7	0x0FDC	Peripheral ID Register 7	0x0000_0000
PID0	0x0FE0	*Peripheral ID Register 0 [7:0] Part number[7:0]	0x0000_0022
PID1	0x0FE4	*Peripheral ID Register 1 [7:4] jep106_id_3_0 [3:0] Part number[11:8]	0x0000_00B8
PID2	0x0FE8	*Peripheral ID Register 2 [7:4] Revision [3] jedec_used [2:0] jep106_id_6_4	0x0000_000B
PID3	0x0FEC	*Peripheral ID Register 3 [7:4] ECO revision number [3:0] customer modification number	0x0000_0000
CID0	0x0FF0	Component ID Register 0	0x0000_000D
CID1	0x0FF4	Component ID Register 1	0x0000_00F0
CID2	0x0FF8	Component ID Register 2	0x0000_0005
CID3	0x0FFC	Component ID Register 3	0x0000_00B1

NOTE: If reserved or empty addresses in the register map are changed, S1SBP6A cannot guarantee normal operation.

4.2.7.1.1.1.1 CTRL

- Base Address: 0x4000_0000
- Address = Base Address + 0x0000, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CTRL	[3:0]	RW	[3] Timer interrupt enable [2] Select external input as clock [1] Select external input as enable [0] Enable	0x0000_0000

4.2.7.1.1.1.2 VALUE

- Base Address: 0x4000_0000
- Address = Base Address + 0x0004, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
VALUE	[31:0]	RW	Current value	0x0000_0000

4.2.7.1.1.1.3 RELOAD

- Base Address: 0x4000_0000
- Address = Base Address + 0x0008, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RELOAD	[31:0]	RW	Reload value. A write to this register sets the current value.	0x0000_0000

4.2.7.1.1.1.4 INTERRUPT

- Base Address: 0x4000_0000
- Address = Base Address + 0x000C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
INTERRUPT	[0]	RW	Write: Timer interrupt. Write 1 to clear this field. Read: Timer interrupt status	0x0000_0000

4.2.7.1.1.1.5 PID4

- Base Address: 0x4000_0000
- Address = Base Address + 0x0FD0, Reset Value = 0x0000_0004

Name	Bit	Type	Description	Reset Value
PID4	[7:0]	R	*Peripheral ID Register 4 [7:4] Block count [3:0] jep106_c_code	0x0000_0004

4.2.7.1.1.1.6 PID5

- Base Address: 0x4000_0000
- Address = Base Address + 0x0FD4, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
PID5	[7:0]	R	Peripheral ID Register 5	0x0000_0000

4.2.7.1.1.1.7 PID6

- Base Address: 0x4000_0000
- Address = Base Address + 0x0FD8, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
PID6	[7:0]	R	Peripheral ID Register 6	0x0000_0000

4.2.7.1.1.1.8 PID7

- Base Address: 0x4000_0000
- Address = Base Address + 0x0FDC, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
PID7	[7:0]	R	Peripheral ID Register 7	0x0000_0000

4.2.7.1.1.1.9 PID0

- Base Address: 0x4000_0000
- Address = Base Address + 0x0FE0, Reset Value = 0x0000_0022

Name	Bit	Type	Description	Reset Value
PID0	[7:0]	R	* Peripheral ID Register 0 [7:0] Part number[7:0]	0x0000_0022

4.2.7.1.1.1.10 PID1

- Base Address: 0x4000_0000
- Address = Base Address + 0x0FE4, Reset Value = 0x0000_00B8

Name	Bit	Type	Description	Reset Value
PID1	[7:0]	R	* Peripheral ID Register 1 [7:4] jep106_id_3_0 [3:0] Part number[11:8]	0x0000_00B8

4.2.7.1.1.1.11 PID2

- Base Address: 0x4000_0000
- Address = Base Address + 0x0FE8, Reset Value = 0x0000_000B

Name	Bit	Type	Description	Reset Value
PID2	[7:0]	R	* Peripheral ID Register 2 [7:4] Revision. [3] jedec_used. [2:0] jep106_id_6_4.	0x0000_000B

4.2.7.1.1.1.12 PID3

- Base Address: 0x4000_0000
- Address = Base Address + 0x0FEC, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
PID3	[7:0]	R	* Peripheral ID Register 3 [7:4] ECO revision number [3:0] Customer modification number	0x0000_0000

4.2.7.1.1.1.13 CID0

- Base Address: 0x4000_0000
- Address = Base Address + 0x0FF0, Reset Value = 0x0000_000D

Name	Bit	Type	Description	Reset Value
CID0	[7:0]	R	Component ID Register 0	0x0000_000D

4.2.7.1.1.1.14 CID1

- Base Address: 0x4000_0000
- Address = Base Address + 0x0FF4, Reset Value = 0x0000_00F0

Name	Bit	Type	Description	Reset Value
CID1	[7:0]	R	Component ID Register 1	0x0000_00F0

4.2.7.1.1.1.15 CID2

- Base Address: 0x4000_0000
- Address = Base Address + 0x0FF8, Reset Value = 0x0000_0005

Name	Bit	Type	Description	Reset Value
CID2	[7:0]	R	Component ID Register 2	0x0000_0005

4.2.7.1.1.1.16 CID3

- Base Address: 0x4000_0000
- Address = Base Address + 0x0FFC, Reset Value = 0x0000_00B1

Name	Bit	Type	Description	Reset Value
CID3	[7:0]	R	Component ID Register 3	0x0000_00B1

4.2.7.2 PWM Timer

Basically, features of PWM Timer are the same as those of General Purpose Timer. Additionally, PWM Timer supports PWM function for motor driver.

PWM Timer supports the following features:

- Programmable period and high duration of PWM signal
- DC or AC motor PWM signal generation
- Programmable motor resonant frequency for AC motor

4.2.7.2.1 Register Description

This section describes the register map information and its associated registers.

4.2.7.2.1.1 Register Map Summary

- Base Address: 0x4000_7000

Register	Offset	Description	Reset Value
CTRL	0x0000	[3] Timer interrupt enable [2] Select external input as clock [1] Select external input as enable [0] Enable	0x0000_0000
VALUE	0x0004	Current value	0x0000_0000
RELOAD	0x0008	Reload value. A write to this register sets the current value.	0x0000_0000
INTERRUPT	0x000C	Write: Timer interrupt. Write 1 to clear this bit. Read: Timer interrupt status	0x0000_0000
PWMCTRL	0x0C00	PWM control	0x0000_0005
PWM_PULSE	0x0C04	PWM pulse set	0x0045_B8B6
PID4	0x0FD0	*Peripheral ID Register 4 [7:4] Block count [3:0] jep106_c_code	0x0000_0004
PID5	0x0FD4	Peripheral ID Register 5	0x0000_0000
PID6	0x0FD8	Peripheral ID Register 6	0x0000_0000
PID7	0x0FDC	Peripheral ID Register 7	0x0000_0000
PID0	0x0FE0	*Peripheral ID Register 0 [7:0] Part number[7:0]	0x0000_0022
PID1	0x0FE4	*Peripheral ID Register 1 [7:4] jep106_id_3_0 [3:0] Part number[11:8]	0x0000_00B8
PID2	0x0FE8	*Peripheral ID Register 2 [7:4] Revision [3] jedec_used [2:0] jep106_id_6_4	0x0000_000B
PID3	0x0FEC	*Peripheral ID Register 3 [7:4] ECO revision number [3:0] Customer modification number	0x0000_0000
CID0	0x0FF0	Component ID Register 0	0x0000_000D
CID1	0x0FF4	Component ID Register 1	0x0000_00F0
CID2	0x0FF8	Component ID Register 2	0x0000_0005

Register	Offset	Description	Reset Value
CID3	0x0FFC	Component ID Register 3	0x0000_00B1

NOTE: If reserved or empty addresses in the register map are changed, S1SBP6A cannot guarantee normal operation.

4.2.7.2.1.1.1 CTRL

- Base Address: 0x4000_7000
- Address = Base Address + 0x0000, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CTRL	[3:0]	RW	[3] Timer interrupt enable [2] Select external input as clock [1] Select external input as enable [0] Enable	0x0000_0000

4.2.7.2.1.1.2 VALUE

- Base Address: 0x4000_7000
- Address = Base Address + 0x0004, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
VALUE	[31:0]	RW	Current value	0x0000_0000

4.2.7.2.1.1.3 RELOAD

- Base Address: 0x4000_7000
- Address = Base Address + 0x0008, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RELOAD	[31:0]	RW	Reload value. A write to this register sets the current value.	0x0000_0000

4.2.7.2.1.1.4 INTERRUPT

- Base Address: 0x4000_7000
- Address = Base Address + 0x000C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
INTERRUPT	[0]	RW	Write: Timer interrupt. Write 1 to clear this bit. Read: Timer interrupt status	0x0000_0000

4.2.7.2.1.1.5 PWMCTRL

- Base Address: 0x4000_7000
- Address = Base Address + 0x0C00, Reset Value = 0x0000_0005

Name	Bit	Type	Description	Reset Value
PWM_EN	[3]	RW	PWM enable	0x0000_0000
MOT_SEL	[2]	RW	* Motor select 0 = DC 1 = AC	0x0000_0001
MRF_SEL	[1:0]	RW	* Motor Resonant Frequency (MRF) selection 00: 128 01: 256 10: 512 11: 1024 For example, when PWM frequency = 44.869 kHz and MRF selection = 01, MRF = 44.869 kHz / 256 = 175.27 Hz	0x0000_0001

4.2.7.2.1.1.6 PWM_PULSE

- Base Address: 0x4000_7000
- Address = Base Address + 0x0C04, Reset Value = 0x0045_B8B6

Name	Bit	Type	Description	Reset Value
PWM_HIGH	[23:12]	RW	High duration of pulse. The minimum valid value for High is 1	0x0000_045B
PWM_PERI	[11:0]	RW	Period of pulse. The minimum valid value for PERI is 2. For a 100 MHz main clock, when PERI = 2230 and HIGH = 1115, PWM out = 44.84 kHz and PWM high duration = 1115/100 MHz = 11.15 μs	0x0000_08B6

4.2.7.2.1.1.7 PID4

- Base Address: 0x4000_7000
- Address = Base Address + 0x0FD0, Reset Value = 0x0000_0004

Name	Bit	Type	Description	Reset Value
PID4	[7:0]	R	* Peripheral ID Register 4 [7:4] Block count. [3:0] jep106_c_code	0x0000_0004

4.2.7.2.1.1.8 PID5

- Base Address: 0x4000_7000
- Address = Base Address + 0x0FD4, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
PID5	[7:0]	R	Peripheral ID Register 5	0x0000_0000

4.2.7.2.1.1.9 PID6

- Base Address: 0x4000_7000
- Address = Base Address + 0x0FD8, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
PID6	[7:0]	R	Peripheral ID Register 6	0x0000_0000

4.2.7.2.1.1.10 PID7

- Base Address: 0x4000_7000
- Address = Base Address + 0x0FDC, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
PID7	[7:0]	R	Peripheral ID Register 7	0x0000_0000

4.2.7.2.1.1.11 PID0

- Base Address: 0x4000_7000
- Address = Base Address + 0x0FE0, Reset Value = 0x0000_0022

Name	Bit	Type	Description	Reset Value
PID0	[7:0]	R	* Peripheral ID Register 0 [7:0] Part number[7:0]	0x0000_0022

4.2.7.2.1.1.12 PID1

- Base Address: 0x4000_7000
- Address = Base Address + 0x0FE4, Reset Value = 0x0000_00B8

Name	Bit	Type	Description	Reset Value
PID1	[7:0]	R	* Peripheral ID Register 1 [7:4] jep106_id_3_0 [3:0] Part number[11:8]	0x0000_00B8

4.2.7.2.1.1.13 PID2

- Base Address: 0x4000_7000
- Address = Base Address + 0x0FE8, Reset Value = 0x0000_000B

Name	Bit	Type	Description	Reset Value
PID2	[7:0]	R	* Peripheral ID Register 2 [7:4] Revision [3] jedec_used [2:0] jep106_id_6_4	0x0000_000B

4.2.7.2.1.1.14 PID3

- Base Address: 0x4000_7000
- Address = Base Address + 0x0FEC, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
PID3	[7:0]	R	* Peripheral ID Register 3 [7:4] ECO revision number [3:0] customer modification number	0x0000_0000

4.2.7.2.1.1.15 CID0

- Base Address: 0x4000_7000
- Address = Base Address + 0x0FF0, Reset Value = 0x0000_000D

Name	Bit	Type	Description	Reset Value
CID0	[7:0]	R	Component ID Register 0	0x0000_000D

4.2.7.2.1.1.16 CID1

- Base Address: 0x4000_7000
- Address = Base Address + 0x0FF4, Reset Value = 0x0000_00F0

Name	Bit	Type	Description	Reset Value
CID1	[7:0]	R	Component ID Register 1	0x0000_00F0

4.2.7.2.1.1.17 CID2

- Base Address: 0x4000_7000
- Address = Base Address + 0x0FF8, Reset Value = 0x0000_0005

Name	Bit	Type	Description	Reset Value
CID2	[7:0]	R	Component ID Register 2	0x0000_0005

4.2.7.2.1.1.18 CID3

- Base Address: 0x4000_7000
- Address = Base Address + 0x0FFC, Reset Value = 0x0000_00B1

Name	Bit	Type	Description	Reset Value
CID3	[7:0]	R	Component ID Register 3	0x0000_00B1

4.2.7.3 Dual-Input Timer

S1SBP6A utilizes dual-input timer of CMSDK (ARM DDI 0479B r0p0). Dual-input timer consists of two programmable 32 bits or 16 bits down-counters that can generate interrupts when they reach 0. It can be used as 32 bits or a 16 bits counter with one of the following timer modes:

- Free-running
- Periodic
- One-shot

The operation of each timer module is identical. Dual-input timer provides access to two interrupt-generating, programmable 32 bits Free-Running Counters (FRCs). The FRCs operate from a common timer clock. Each FRC also has a prescaler that can divide down the common timer clock rate by 1, 16, or 256. This enables the count rate for each FRC.

'The system clock is a gated APB clock (PCLK) which controls the programmable registers, and the second clock input is an APB clock (TIMCLK) which drives the counter.

Figure 4-10 illustrates a top-level block diagram of the dual-input timers.

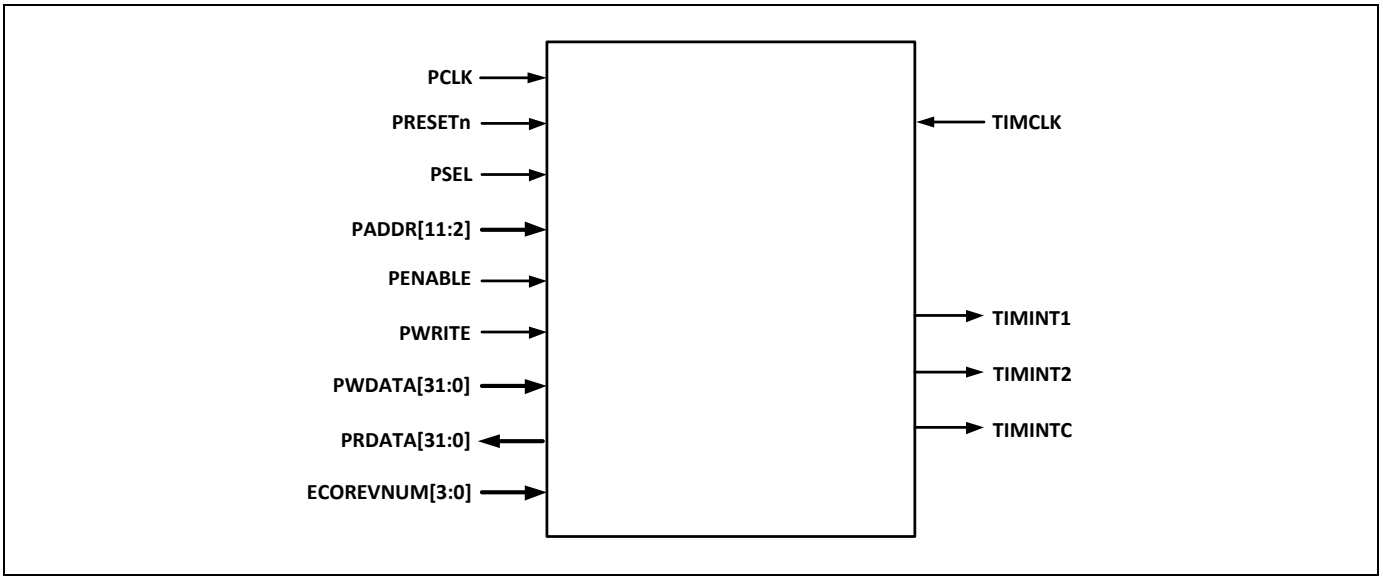


Figure 4-10 Dual-Input Timer Components

4.2.7.3.1 Functional Description

Two timers are defined by default, although you can easily expand this through extra instantiations of the FRC block. The same principle of simple expansion has been applied to the register configuration, to enable you to use more complex counters. For each timer, the following modes of operation are available:

Free-Running Mode

The counter wraps after reaching its zero value, and continues to count down from the maximum value. It is the default mode.

Periodic Timer Mode

The counter generates an interrupt at a constant interval, reloading the original value after counter reaches zero.

One-Shot Timer Mode

The counter generates an interrupt only once. When the counter reaches 0, it halts until you reprogram it. You can achieve this by either clearing the one-shot count bit in the control register so that the count proceeds according to the selection of Free-running or Periodic mode or writing a new value to the Load Value register.

4.2.7.3.2 Operation of Dual-Input Timer

Each timer has an identical set of registers. The operation of each timer is identical. The timer is loaded by writing to the load register and, if enabled, counts down to 0. When a counter is already running, writing to the load register causes the counter to immediately restart at the new value. Writing to the background load value has no effect on the current count. The counter continues to decrement to 0, and then recommences from the new load value, if in periodic mode, and one-shot mode is not selected.

When 0 is reached, an interrupt is generated. You can clear the interrupt by writing to the clear register. If one-shot mode is selected, the counter halts when it reaches 0 until you deselect one-shot mode, or write a new load value. Otherwise, after reaching a zero count, if the timer is operating in free-running mode, it continues to decrement from its maximum value. If periodic timer mode is selected, the timer reloads the count value from the Load register and continues to decrement. In this mode, the counter effectively generates a periodic interrupt.

You select the mode using a bit in the Timer Control register. At any point, you can read the current counter value from the Current Value register. You can enable the counter using a bit in the control register.

At reset, the counter is disabled, the interrupt is cleared, and the load register is set to 0. The mode and prescale values are set to free-running and clock divide of one respectively.

Figure 4-11 illustrates a block diagram of the free-running timer module.

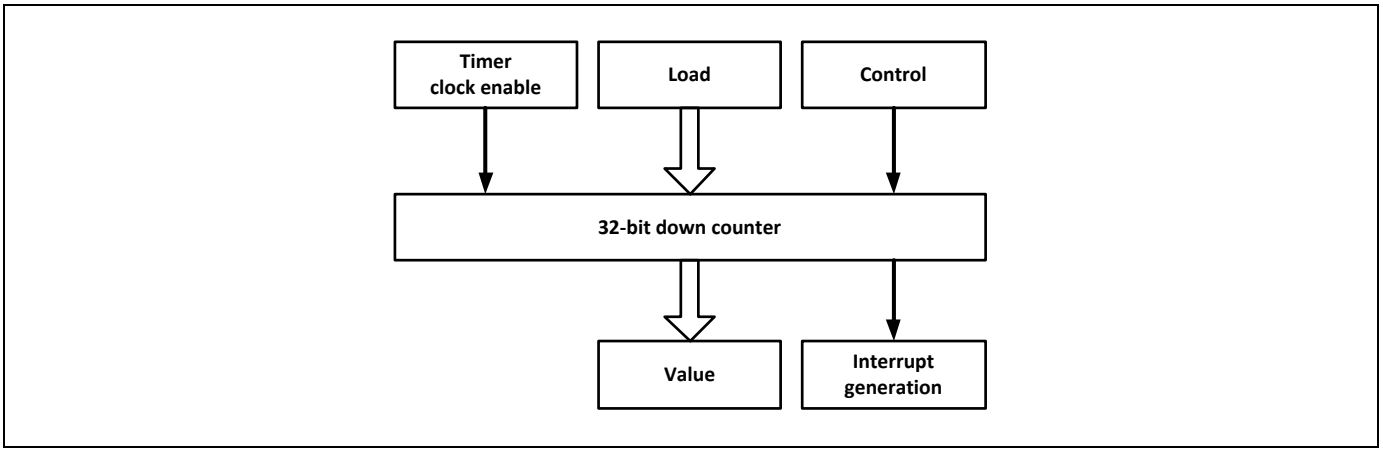


Figure 4-11 Free-Running Timer Block

The timer clock enable is generated by a prescale unit. The counter then uses the enable to create a clock with one of the following timings:

- The system clock
- The system clock divided by 16 and generated by 4 bits of prescale
- The system clock divided by 256 and generated by a total of 8 bits of prescale

Figure 4-12 illustrates how the timer clock frequency is selected in the prescale unit. This enables you to clock the timer at different frequencies.

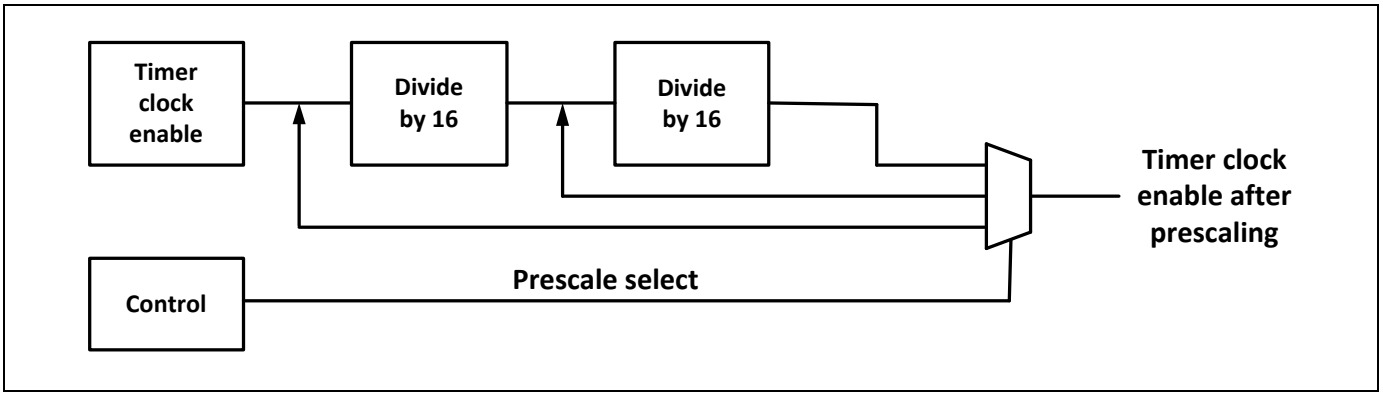


Figure 4-12 Prescale Clock Enable Generation

An interrupt is generated when the full 32 bits counter reaches 0, and is only cleared when the TimerXClear location is written to. A register holds the value until the interrupt is cleared. The most significant carry bit of the counter detects the counter reaching 0.

You can mask interrupts by writing 0 to the Interrupt Enable bit in the Control Register. You can read the following from status registers:

- Raw interrupt status, prior to masking
- Final interrupt status, after masking.

The interrupts from the individual counters, after masking, are logically ORed into a combined interrupt, TIMINTC, and this provides an additional output from the timer peripheral.

4.2.7.3.3 Clocking

The timers contain the PCLK and TIMCLK clock inputs, and the clocks are synchronous. PCLK is APB gated clock and the register interface uses it. TIMCLK is the APB system clock. TIMCLK is the input to the prescale units and the decrementing counters.

4.2.7.3.4 Register Description

This section describes the register map information and its associated registers.

4.2.7.3.4.1 Register Map Summary

- Base Address: 0x4000_8000

Register	Offset	Description	Reset Value
TIMER1LOAD	0x0000	Timer Load value replaces the current count value	0x0000_0000
TIMER1VALUE	0x0004	Provides the current value of the decrementing counter	0xFFFF_FFFF
TIMER1CONTROL	0x0008	Timer1 control register	0x0000_0020
TIMER1INTCLR	0x000C	Clears the interrupt output from the counter	0x0000_0000
TIMER1RIS	0x0010	Raw interrupt status from the counter	0x0000_0000
TIMER1MIS	0x0014	Enabled interrupt status from the counter	0x0000_0000
TIMER1BGLOAD	0x0018	This is the value used to reload the counter when Periodic mode is enabled and the current count reaches 0.	0x0000_0000
TIMER2LOAD	0x0020	Timer Load value replaces the current count value	0x0000_0000
TIMER2VALUE	0x0024	Provides the current value of the decrementing counter	0xFFFF_FFFF
TIMER2CONTROL	0x0028	The same as TIMER1CONTROL	0x0000_0020
TIMER2INTCLR	0x002C	Clears the interrupt output from the counter	0x0000_0000
TIMER2RIS	0x0030	Raw interrupt status from the counter	0x0000_0000
TIMER2MIS	0x0034	Enabled interrupt status from the counter	0x0000_0000
TIMER2BGLOAD	0x0038	This is the value used to reload the counter when Periodic mode is enabled and the current count reaches 0	0x0000_0000
TIMERPERIOHID4	0x0FD0	*Peripheral ID Register 4 [7:4] Block count	0x0000_0004

Register	Offset	Description	Reset Value
		[3:0] jep106_c_code	
TIMERPERIOHID5	0x0FD4	Peripheral ID Register 5	0x0000_0000
TIMERPERIPHID6	0x0FD8	Peripheral ID Register 6	0x0000_0000
TIMERPERIPHID7	0x0FDC	Peripheral ID Register 7	0x0000_0000
TIMERPERIPHID0	0x0FE0	*Peripheral ID Register 0 [7:0] Part number[7:0]	0x0000_0023
TIMERPERIPHID1	0x0FE4	*Peripheral ID Register 1 [7:4] jep106_id_3_0 [3:0] Part number[11:8]	0x0000_00B8
TIMERPERIPHID2	0x0FE8	*Peripheral ID Register 2 [7:4] Revision [3] jedec_used [2:0] jep106_id_6_4	0x0000_000B
TIMERPERIPHID3	0x0FEC	*Peripheral ID Register 3: [7:4] ECO revision number [3:0] Customer modification number	0x0000_0000
TIMERPCELLID0	0x0FF0	Component ID Register 0	0x0000_000D
TIMERPCELLID1	0x0FF4	Component ID Register 1	0x0000_00F0
TIMERPCELLID2	0x0FF8	Component ID Register 2	0x0000_0005
TIMERPCELLID3	0x0FFC	Component ID Register 3	0x0000_00B1

NOTE: If reserved or empty addresses in the register map are changed, S1SBP6A cannot guarantee normal operation.

4.2.7.3.4.1.1 TIMER1LOAD

- Base Address: 0x4000_8000
- Address = Base Address + 0x0000, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
TIMER1LOAD	[31:0]	RW	Timer Load value replaces the current count value	0x0000_0000

4.2.7.3.4.1.2 TIMER1VALUE

- Base Address: 0x4000_8000
- Address = Base Address + 0x0004, Reset Value = 0x0FFF_FFFF

Name	Bit	Type	Description	Reset Value
TIMER1VALUE	[31:0]	R	Provides the current value of the decrementing counter	0xFFFF_FFFF

4.2.7.3.4.1.3 TIMER1CONTROL

- Base Address: 0x4000_8000
- Address = Base Address + 0x0008, Reset Value = 0x0000_0020

Name	Bit	Type	Description	Reset Value
TimerEnable	[7]	RW	* Enable bit 0 = Timer disabled (default) 1 = Timer enabled	0x0000_0000
TimerMode	[6]	RW	* Mode bit 0 = Timer is in free-running mode (default) 1 = Timer is in periodic mode	0x0000_0000
InterruptEnable	[5]	RW	* Interrupt Enable bit 0 = Timer interrupt disabled 1 = Timer interrupt enabled (default)	0x0000_0001
RESERVED	[4]	RW	Reserved bit. Do not modify and ignore on read.	0x0000_0000
TimerPre	[3:2]	RW	* Prescale bits: 00: 0 stages of prescale. clock is divided by 1 (default) 01: 4 stages of prescale. clock is divided by 16 10: 8 stages of prescale. clock is divided by 256 11: Undefined. Do not use.	0x0000_0000
TimerSize	[1]	RW	* Selects 16 or 32 bits counter operation 0 = 16 bits counter (default) 1 = 32 bits counter	0x0000_0000
OneshortCount	[0]	RW	* Selects one-shot or wrapping counter mode 0 = Wrapping mode (default) 1 = One-shot mode	0x0000_0000

4.2.7.3.4.1.4 TIMER1INTCLR

- Base Address: 0x4000_8000
- Address = Base Address + 0x000C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
TIMER1INTCLR	[0]	W	Clears the interrupt output from the counter	0x0000_0000

4.2.7.3.4.1.5 TIMER1RIS

- Base Address: 0x4000_8000
- Address = Base Address + 0x0010, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
TIMER1RIS	[0]	R	Raw interrupt status from the counter	0x0000_0000

4.2.7.3.4.1.6 TIMER1MIS

- Base Address: 0x4000_8000
- Address = Base Address + 0x0014, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
TIMER1MIS	[0]	R	Enabled interrupt status from the counter	0x0000_0000

4.2.7.3.4.1.7 TIMER1BGLOAD

- Base Address: 0x4000_8000
- Address = Base Address + 0x0018, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
TIMER1BGLOAD	[31:0]	RW	The value used to reload the counter when Periodic mode is enabled and the current count reaches 0.	0x0000_0000

4.2.7.3.4.1.8 TIMER2LOAD

- Base Address: 0x4000_8000
- Address = Base Address + 0x0020, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
TIMER2LOAD	[31:0]	RW	Timer Load value replaces the current count value	0x0000_0000

4.2.7.3.4.1.9 TIMER2VALUE

- Base Address: 0x4000_8000
- Address = Base Address + 0x0024, Reset Value = 0x0FFF_FFFF

Name	Bit	Type	Description	Reset Value
TIMER2VALUE	[31:0]	R	Provides the current value of the decrementing counter	0xFFFF_FFFF

4.2.7.3.4.1.10 TIMER2CONTROL

- Base Address: 0x4000_8000
- Address = Base Address + 0x0028, Reset Value = 0x0000_0020

Name	Bit	Type	Description	Reset Value
TIMER2CONTROL	[7:0]	RW	The same as TIMER1CONTROL	0x0000_0020

4.2.7.3.4.1.11 TIMER2INTCLR

- Base Address: 0x4000_8000
- Address = Base Address + 0x002C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
TIMER2INTCLR	[0]	W	Clears the interrupt output from the counter	0x0000_0000

4.2.7.3.4.1.12 TIMER2RIS

- Base Address: 0x4000_8000
- Address = Base Address + 0x0030, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
TIMER2RIS	[0]	R	Raw interrupt status from the counter	0x0000_0000

4.2.7.3.4.1.13 TIMER2MIS

- Base Address: 0x4000_8000
- Address = Base Address + 0x0034, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
TIMER2MIS	[0]	R	Enabled interrupt status from the counter	0x0000_0000

4.2.7.3.4.1.14 TIMER2BGLOAD

- Base Address: 0x4000_8000
- Address = Base Address + 0x0038, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
TIMER2BGLOAD	[31:0]	RW	The value used to reload the counter when Periodic mode is enabled and the current count reaches 0.	0x0000_0000

4.2.7.3.4.1.15 TIMERPERIOHID4

- Base Address: 0x4000_8000
- Address = Base Address + 0x0FD0, Reset Value = 0x0000_0004

Name	Bit	Type	Description	Reset Value
TIMERPERIOHID4	[7:0]	R	* Peripheral ID Register 4 [7:4] Block count [3:0] jep106_c_code	0x0000_0004

4.2.7.3.4.1.16 TIMERPERIOHID5

- Base Address: 0x4000_8000
- Address = Base Address + 0x0FD4, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
TIMERPERIOHID5	[7:0]	R	Peripheral ID Register 5	0x0000_0000

4.2.7.3.4.1.17 TIMERPERIPHID6

- Base Address: 0x4000_8000
- Address = Base Address + 0x0FD8, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
TIMERPERIPHID6	[7:0]	R	Peripheral ID Register 6	0x0000_0000

4.2.7.3.4.1.18 TIMERPERIPHID7

- Base Address: 0x4000_8000
- Address = Base Address + 0x0FDC, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
TIMERPERIPHID7	[7:0]	R	Peripheral ID Register 7	0x0000_0000

4.2.7.3.4.1.19 TIMERPERIPHID0

- Base Address: 0x4000_8000
- Address = Base Address + 0x0FE0, Reset Value = 0x0000_0023

Name	Bit	Type	Description	Reset Value
TIMERPERIPHID0	[7:0]	R	* Peripheral ID Register 0 [7:0] Part number[7:0]	0x0000_0023

4.2.7.3.4.1.20 TIMERPERIPHID1

- Base Address: 0x4000_8000
- Address = Base Address + 0x0FE4, Reset Value = 0x0000_00B8

Name	Bit	Type	Description	Reset Value
TIMERPERIPHID1	[7:0]	R	* Peripheral ID Register 1 [7:4] jep106_id_3_0 [3:0] Part number[11:8]	0x0000_00B8

4.2.7.3.4.1.21 TIMERPERIPHID2

- Base Address: 0x4000_8000
- Address = Base Address + 0x0FE8, Reset Value = 0x0000_000B

Name	Bit	Type	Description	Reset Value
TIMERPERIPHID2	[7:0]	R	* Peripheral ID Register 2 [7:4] Revision [3] jedec_used [2:0] jep106_id_6_4	0x0000_000B

4.2.7.3.4.1.22 TIMERPERIPHID3

- Base Address: 0x4000_8000
- Address = Base Address + 0x0FEC, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
TIMERPERIPHID3	[7:0]	R	* Peripheral ID Register 3 [7:4] ECO revision number [3:0] customer modification number	0x0000_0000

4.2.7.3.4.1.23 TIMERPCELLID0

- Base Address: 0x4000_8000
- Address = Base Address + 0x0FF0, Reset Value = 0x0000_000D

Name	Bit	Type	Description	Reset Value
TIMERPCELLID0	[7:0]	R	Component ID Register 0	0x0000_000D

4.2.7.3.4.1.24 TIMERPCELLID1

- Base Address: 0x4000_8000
- Address = Base Address + 0x0FF4, Reset Value = 0x0000_00F0

Name	Bit	Type	Description	Reset Value
TIMERPCELLID1	[7:0]	R	Component ID Register 1	0x0000_00F0

4.2.7.3.4.1.25 TIMERPCELLID2

- Base Address: 0x4000_8000
- Address = Base Address + 0x0FF8, Reset Value = 0x0000_0005

Name	Bit	Type	Description	Reset Value
TIMERPCELLID2	[7:0]	R	Component ID Register 2	0x0000_0005

4.2.7.3.4.1.26 TIMERPCELLID3

- Base Address: 0x4000_8000
- Address = Base Address + 0x0FFC, Reset Value = 0x0000_00B1

Name	Bit	Type	Description	Reset Value
TIMERPCELLID3	[7:0]	R	Component ID Register 3	0x0000_00B1

4.2.7.4 Watchdog

S1SBP6A utilizes Watchdog of CMSDK (ARM DDI 0479B r0p0). Watchdog is based on a 32 bits down-counter that is initialized from the Reload register. Watchdog generates a regular interrupt depending on a programmed value. The counter decrements by one on each positive clock edge of Watchdog clock.

Watchdog monitors the interrupt and asserts a reset signal when the counter reaches 0 and the counter stops. On the next Watchdog clock edge, the counter is reloaded from the Load register and the count-down sequence continues. If the interrupt is not cleared by the time the counter reaches 0 again, then Watchdog reasserts the reset signal. Watchdog applies a reset to the system during software failure to recover from software crashes.

Figure 4-13 illustrates the watchdog module.

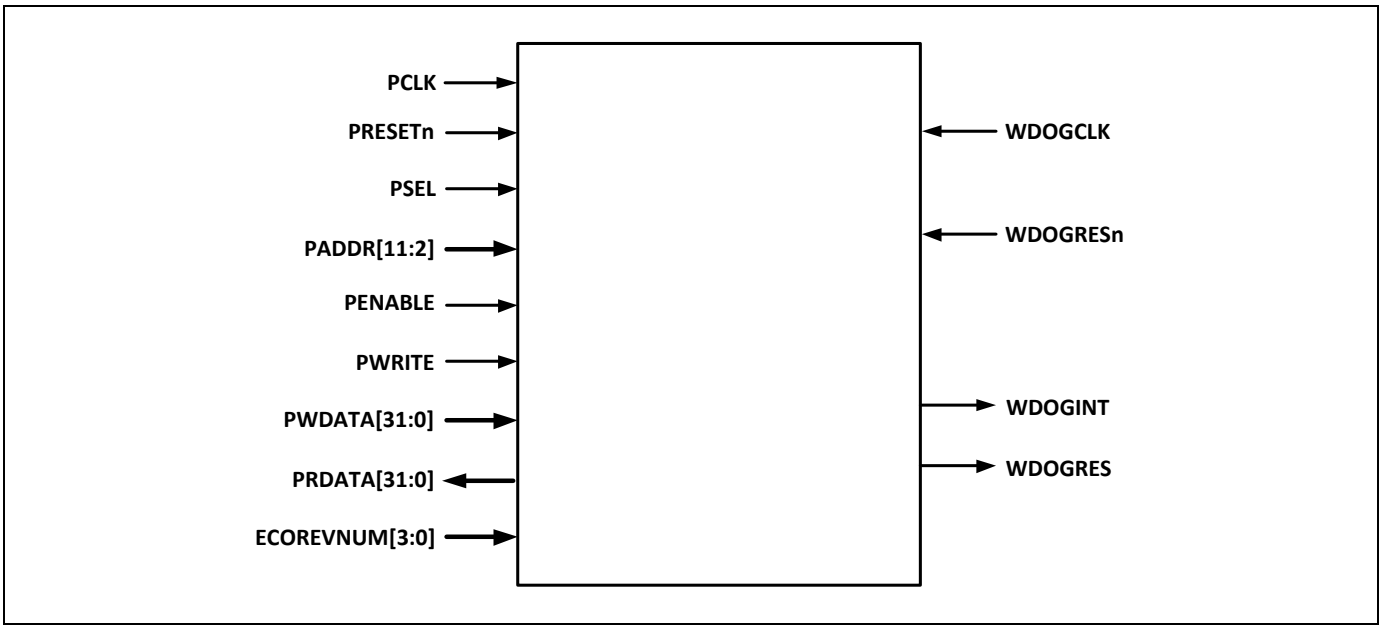


Figure 4-13 Watchdog Components

Figure 4-14 illustrates the flow diagram for watchdog operation.

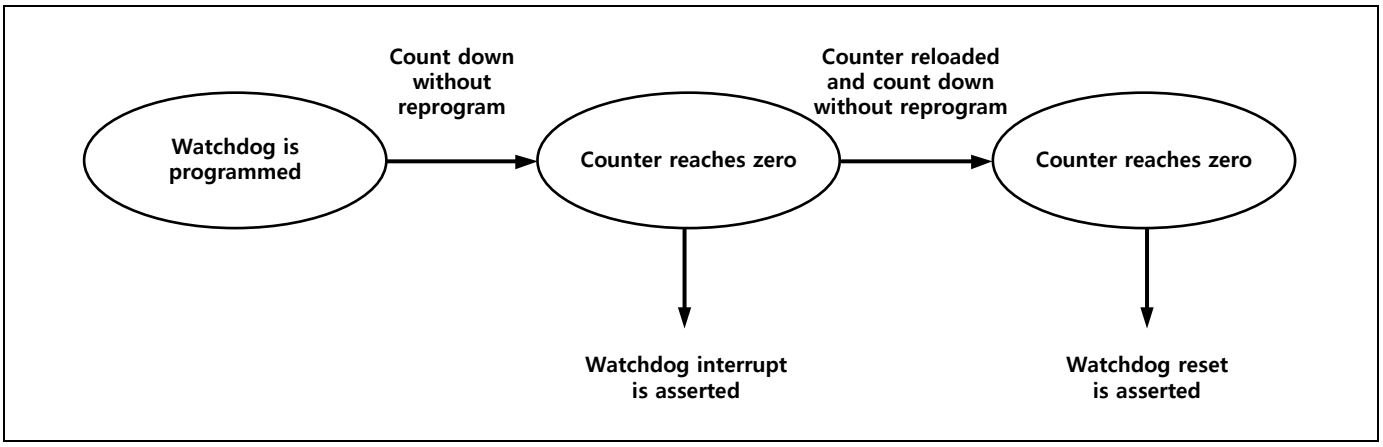


Figure 4-14 Flow Diagram for Watchdog Operation

4.2.7.4.1 Register Description

This section describes the register map information and its associated registers.

4.2.7.4.1.1 Register Map Summary

- Base Address: 0x4000_9000

Register	Offset	Description	Reset Value
WDOGLOAD	0x0000	A 32-bit register that contains the value from which the counter is being decremented. A write of any value to this register reloads the counter from the new value and restarts the counter. The minimum valid value for WDOGLOAD is 1.	0xFFFF_FFFF
WDOGVALUE	0x0004	Provides the current value of the decrementing counter.	0xFFFF_FFFF
WDOGCONTROL	0x0008	A R/W register that enables the software to control the watchdog unit.	0x0000_0000
WDOGINTCLR	0x000C	A write of any value to this register clears the watchdog interrupt and reloads the counter from the value in WDOGLOAD.	0x0000_0000
WDOGRIS	0x0010	Raw interrupt status from the counter. This value is ANDed with the interrupt enable bit from the control register to create the masked interrupt that is passed to the interrupt output pin.	0x0000_0000
WDOGMIS	0x0014	Enabled interrupt status from the counter. It indicates the masked interrupt status from the counter. This value is the logical AND of the raw interrupt status with the INTEN bit from the control register and is the same value that is passed to the interrupt output pin.	0x0000_0000
WDOGLOCK	0x0C00	Write-only register. Using this register disables the write-accesses to all other registers. This is to prevent rogue software from disabling the watchdog functionality. Writing a value of 0x1ACCE551 enables write access to all other registers. Writing any other value disables write accesses.	0x0000_0000
WDOGPERIPHID4	0x0FD0	*Peripheral ID Register 4 [7:4] Block count [3:0] jep106_c_code	0x0000_0004
WDOGPERIPHID5	0x0FD4	Peripheral ID Register 5	0x0000_0000
WDOGPERIPHID6	0x0FD8	Peripheral ID Register 6	0x0000_0000
WDOGPERIPHID7	0x0FDC	Peripheral ID Register 7	0x0000_0000
WDOGPERIPHID0	0x0FE0	*Peripheral ID Register 0 [7:0] Part number[7:0]	0x0000_0024
WDOGPERIPHID1	0x0FE4	*Peripheral ID Register 1 [7:4] jep106_id_3_0	0x0000_00B8

Register	Offset	Description	Reset Value
		[3:0] Part number[11:8]	
WDOGPERIPHID2	0x0FE8	*Peripheral ID Register 2 [7:4] Revision [3] jedec_used [2:0] jep106_id_6_4	0x0000_000B
WDOGPERIPHID3	0x0FEC	*Peripheral ID Register 3 [7:4] ECO revision number [3:0] Customer modification number	0x0000_0000
WDOGPCELLID0	0x0FF0	Component ID Register 0	0x0000_000D
WDOGPCELLID1	0x0FF4	Component ID Register 1	0x0000_00F0
WDOGPCELLID2	0x0FF8	Component ID Register 2	0x0000_0005
WDOGPCELLID3	0x0FFC	Component ID Register 3	0x0000_00B1

NOTE: If reserved or empty addresses in the register map are changed, S1SBP6A cannot guarantee normal operation.

4.2.7.4.1.1.1 WDOGLOAD

- Base Address: 0x4000_9000
- Address = Base Address + 0x0000, Reset Value = 0x0FFF_FFFF

Name	Bit	Type	Description	Reset Value
WDOGLOAD	[31:0]	RW	The WDOGLOAD Register is a 32 bits register containing the value from which the counter is to decrement. When this register is written to the count is immediately restarted from the new value. The minimum valid value for WDOGLOAD is 1.	0xFFFF_FFFF

4.2.7.4.1.1.2 WDOGVALUE

- Base Address: 0x4000_9000
- Address = Base Address + 0x0004, Reset Value = 0x0FFF_FFFF

Name	Bit	Type	Description	Reset Value
WDOGVALUE	[31:0]	R	The WDOGVALUE Register gives the current value of the decrementing counter.	0xFFFF_FFFF

4.2.7.4.1.1.3 WDOGCONTROL

- Base Address: 0x4000_9000
- Address = Base Address + 0x0008, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RESEN	[1]	RW	Enable watchdog reset output WDOGRE. Acts as a mask for the reset output. High: Enables the reset Low: Disables the reset	0x0000_0000
INTEN	[0]	RW	Enable the interrupt event WDOGINT. High: Enables the counter and interrupt Low: Disables the counter and interrupt. Reloads the counter from the value in WDOGLOAD when the interrupt is enabled and was previously disabled.	0x0000_0000

4.2.7.4.1.1.4 WDOGINTCLR

- Base Address: 0x4000_9000
- Address = Base Address + 0x000C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
WDOGINTCLR	[0]	W	A write of any value to the WDOGINTCLR Register clears the watchdog interrupt and reloads the counter from the value in WDOGLOAD.	0x0000_0000

4.2.7.4.1.1.5 WDOGRIS

- Base Address: 0x4000_9000
- Address = Base Address + 0x0010, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
WDOGRIS	[0]	R	Raw interrupt status from the counter. This value is ANDed with the interrupt enable bit from the control register to create the masked interrupt that is passed to the interrupt output pin.	0x0000_0000

4.2.7.4.1.1.6 WDOGMIS

- Base Address: 0x4000_9000
- Address = Base Address + 0x0014, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
WDOGMIS	[0]	R	Enabled interrupt status from the counter. It indicates the masked interrupt status from the counter. This value is the logical AND of the raw interrupt status with the INTEN bit from the control register and is the same value that is passed to the interrupt output pin.	0x0000_0000

4.2.7.4.1.1.7 WDOGLOCK

- Base Address: 0x4000_9000
- Address = Base Address + 0x0C00, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
WDOGLOCK	[31:0]	RW	The WDOGLOCK Register is write-only. Using this register disables the write-accesses to all other registers. This is to prevent rogue software from disabling the watchdog functionality. Writing a value of 0x1ACCE551 enables write access to all other registers. Writing any other value disables write accesses. A read from this register returns only the bottom bit: 0 = Indicates that write access is enabled (not locked) 1 = Indicates that write access is disabled (locked)	0x0000_0000

4.2.7.4.1.1.8 WDOGPERIPHID4

- Base Address: 0x4000_9000
- Address = Base Address + 0x0FD0, Reset Value = 0x0000_0004

Name	Bit	Type	Description	Reset Value
WDOGPERIPHID4	[7:0]	R	* Peripheral ID Register 4 [7:4] Block count [3:0] jep106_c_code	0x0000_0004

4.2.7.4.1.1.9 WDOGPERIPHID5

- Base Address: 0x4000_9000
- Address = Base Address + 0x0FD4, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
WDOGPERIPHID5	[7:0]	R	Peripheral ID Register 5	0x0000_0000

4.2.7.4.1.1.10 WDOGPERIPHID6

- Base Address: 0x4000_9000
- Address = Base Address + 0x0FD8, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
WDOGPERIPHID6	[7:0]	R	Peripheral ID Register 6	0x0000_0000

4.2.7.4.1.1.11 WDOGPERIPHID7

- Base Address: 0x4000_9000
- Address = Base Address + 0x0FDC, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
WDOGPERIPHID7	[7:0]	R	Peripheral ID Register 7	0x0000_0000

4.2.7.4.1.1.12 WDOGPERIPHID0

- Base Address: 0x4000_9000
- Address = Base Address + 0x0FE0, Reset Value = 0x0000_0024

Name	Bit	Type	Description	Reset Value
WDOGPERIPHID0	[7:0]	R	* Peripheral ID Register 0 [7:0] Part number[7:0]	0x0000_0024

4.2.7.4.1.1.13 WDOGPERIPHID1

- Base Address: 0x4000_9000
- Address = Base Address + 0x0FE4, Reset Value = 0x0000_00B8

Name	Bit	Type	Description	Reset Value
WDOGPERIPHID1	[7:0]	R	Peripheral ID Register 1 [7:4] jep106_id_3_0 [3:0] Part number[11:8]	0x0000_00B8

4.2.7.4.1.1.14 WDOGPERIPHID2

- Base Address: 0x4000_9000
- Address = Base Address + 0x0FE8, Reset Value = 0x0000_000B

Name	Bit	Type	Description	Reset Value
WDOGPERIPHID2	[7:0]	R	Peripheral ID Register 2 [7:4] Revision [3] jedec_used [2:0] jep106_id_6_4	0x0000_000B

4.2.7.4.1.1.15 WDOGPERIPHID3

- Base Address: 0x4000_9000
- Address = Base Address + 0x0FEC, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
WDOGPERIPHID3	[7:0]	R	Peripheral ID Register 3 [7:4] ECO revision number [3:0] Customer modification number	0x0000_0000

4.2.7.4.1.1.16 WDOGPCELLID0

- Base Address: 0x4000_9000
- Address = Base Address + 0x0FF0, Reset Value = 0x0000_000D

Name	Bit	Type	Description	Reset Value
WDOGPCELLID0	[7:0]	R	Component ID Register 0	0x0000_000D

4.2.7.4.1.1.17 WDOGPCELLID1

- Base Address: 0x4000_9000
- Address = Base Address + 0x0FF4, Reset Value = 0x0000_00F0

Name	Bit	Type	Description	Reset Value
WDOGPCELLID1	[7:0]	R	Component ID Register 1	0x0000_00F0

4.2.7.4.1.1.18 WDOGPCELLID2

- Base Address: 0x4000_9000
- Address = Base Address + 0x0FF8, Reset Value = 0x0000_0005

Name	Bit	Type	Description	Reset Value
WDOGPCELLID2	[7:0]	R	Component ID Register 2	0x0000_0005

4.2.7.4.1.1.19 WDOGPCELLID3

- Base Address: 0x4000_9000
- Address = Base Address + 0x0FFC, Reset Value = 0x0000_00B1

Name	Bit	Type	Description	Reset Value
WDOGPCELLID3	[7:0]	R	Component ID Register 3	0x0000_00B1

4.2.8 Universal Asynchronous Receiver Transmitter

Universal Asynchronous Receiver Transmitter (UART) supports three independent UART channels with asynchronous and serial input/output ports for general purpose.

UART supports the following features:

- Channel 0 to 2 with 64-byte FIFO
- All channels with interrupt-based operation
- All channels with DMA-based or interrupt-based operation
- All channels with auto flow control with nRTS and nCTS
- Handshake transmit/receive

Each UART channel contains two FIFOs to receive and transmit data, a Baud-rate generator, a transmitter, a receiver and a control unit. The Baud-rate generator uses EXT_UCLK. The transmitter and the receiver contain FIFOs and data shifters. The data that is transmitted is written to TX FIFO and copied to the transmit shifter. The data is then shifted out by the transmit data pin (TxDn). The received data is shifted from the Receive Data Pin (RxDn), and copied to RX FIFO from the shifter.

Figure 4-15 illustrates the UART module, *Figure 4-16* illustrates a top-level block diagram of the UART, and *Figure 4-17* illustrates the data flow of UART.

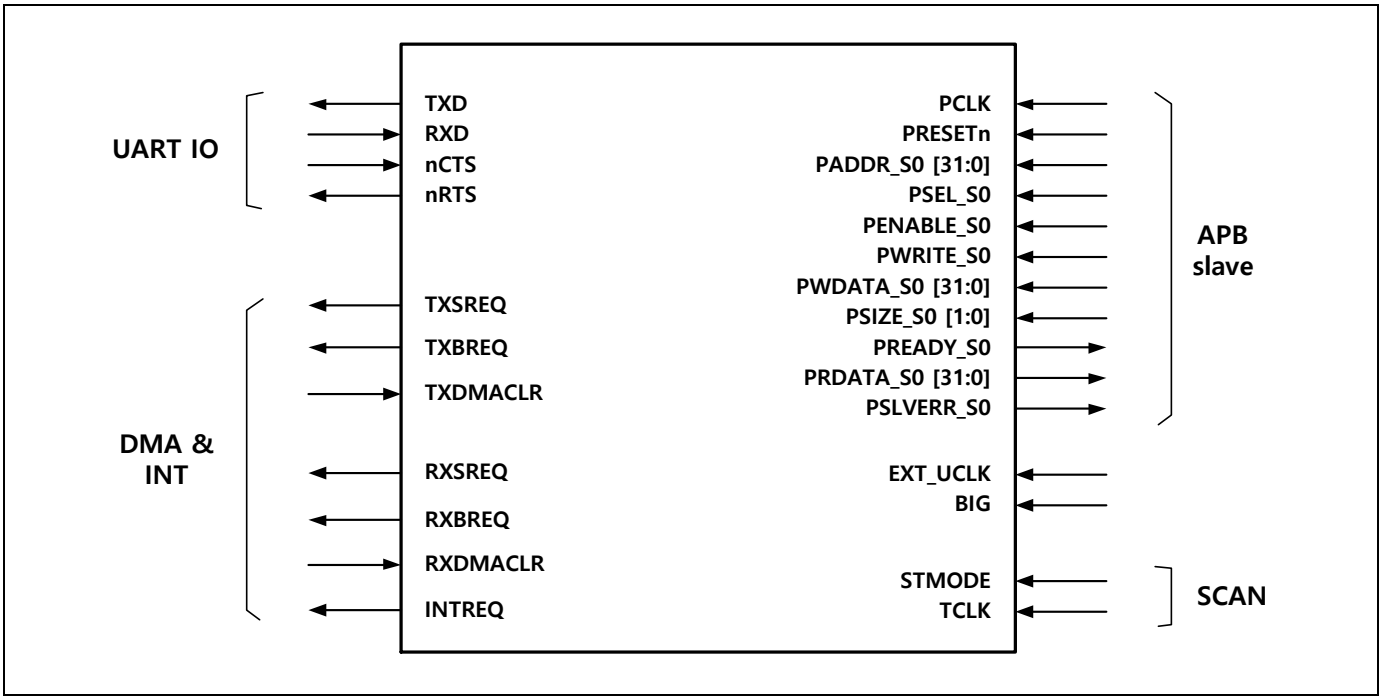


Figure 4-15 UART Components

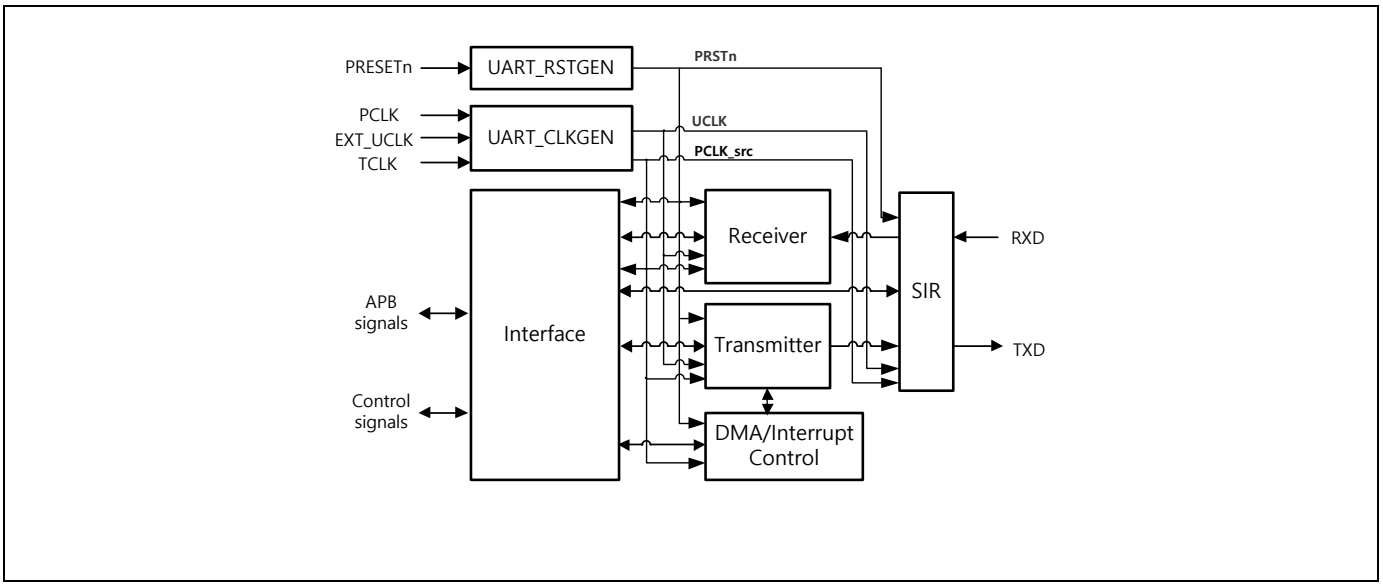


Figure 4-16 Block Diagram of UART

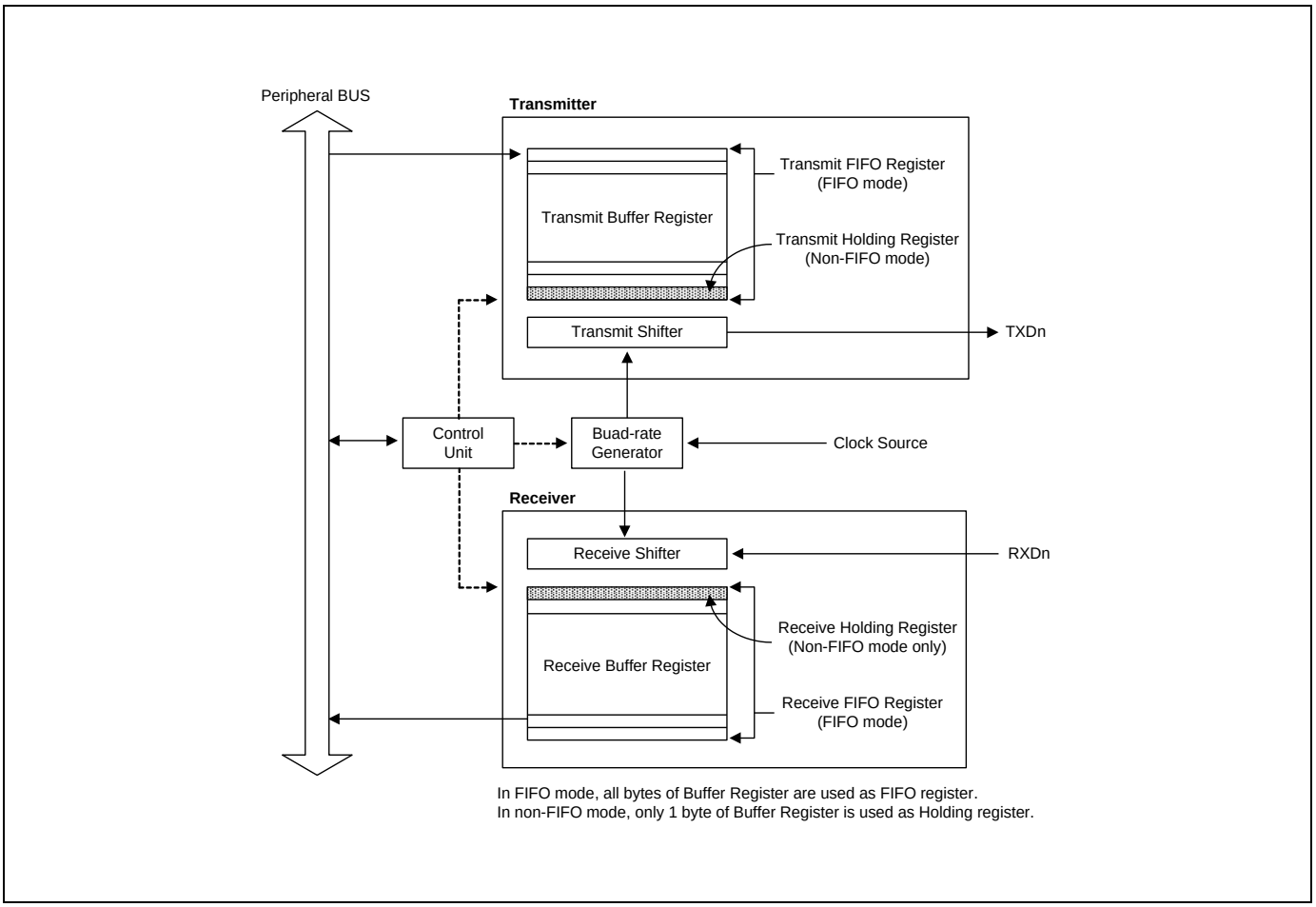


Figure 4-17 Data Flow of UART

4.2.8.1 Functional Description

This section describes UART operations, such as data transmission, data reception, interrupt/DMA request generation and auto flow control.

4.2.8.1.1 Data Transmission

The data frame for transmission is programmable. It consists of a start bit, five to eight data bits, an optional parity bit, and one to two stop bits, specified by the line control register (ULCONn). The transmitter can also produce a break condition that forces the serial output to logic 0 state for one frame transmission time. This block transmits the break signals after the present transmission word is transmitted completely. After the break signal transmission, the transmitter continuously transmits data to TX FIFO (TX holding register, in case of non-FIFO mode).

4.2.8.1.2 Data Reception

Similar to data transmission, the data frame for reception is also programmable. It consists of a start bit, five to eight data bits, an optional parity bit, and one to two stop bits in the Line Control Register (ULCONn). The receiver detects Overrun Error, Parity Error, Frame Error, and Break Condition. Each of this error sets an error flag. Following is the description for each error:

- Overrun Error indicates that new data has overwritten the old data before it was read.
- Parity Error indicates that the receiver has detected an unexpected parity condition.
- Frame Error indicates that the received data does not have a valid stop bit.
- Break Condition indicates that the RxDn input is held in the logic 0 state for more than one frame transmission time.

Receive time-out condition occurs when the RX FIFO is not empty in the FIFO mode and no more data is received during the frame time specified in UCON.

4.2.8.1.3 Auto Flow Control (AFC)

In AFC, the nRTS signal depends on the condition of the receiver, whereas the nCTS signal controls the operation of transmitter. The transmitter of UART transfers the data to FIFO when nCTS signals are activated. Iin AFC, nCTS signals indicate that FIFO of other UART is ready to receive data. Before UART receives data, the nRTS signals must be activated when its Receive FIFO has more than 2-byte as spare. The nRTS signals must be deactivated when its Receive FIFO has less than 1-byte as spare. In AFC, the nRTS signals indicate that its own Receive FIFO is ready to receive data. *Figure 4-18* illustrates the UART AFC Interface.

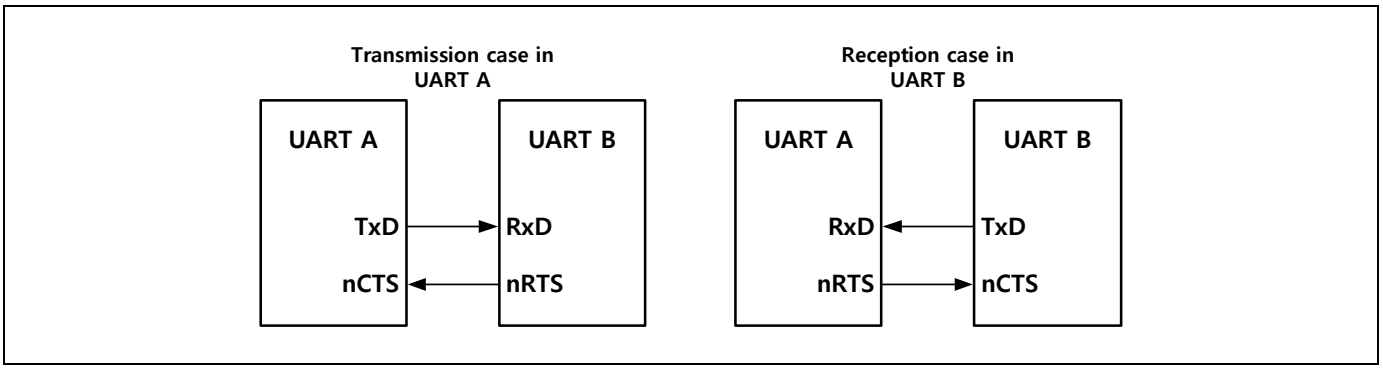


Figure 4-18 UART AFC Interface

4.2.8.1.4 Interrupt/DMA Request Generation

Each UART comprises of seven status (TX/RX/Error) signals such as Overrun Error, Parity Error, Frame Error, Break, Receive Buffer Data Ready, Transmit Buffer Empty, and Transmit Shifter Empty. The corresponding UART status register (UTRSTATn/UERSTATn) indicates these conditions.

The Overrun Error, Parity Error, Frame Error and Break Condition specify the receive error status. When the receive-error-status-interrupt-enable bit is set to 1 in the control register (UCONn), the receive error status generates receive-error-status-interrupt. When a receive-error-status-interrupt-request is detected, you can read the value of UERSTATn to identify the source of interrupt.

When the receiver transfers data of the receive shifter to the receive FIFO register in FIFO mode and the amount of received data is greater than or equal to the RX FIFO trigger level, RX interrupt is generated if Receive mode in control register (UCONn) is set to 1 (Interrupt request or Polling mode).

In non-FIFO mode, transferring the data of receive shifter to receive holding register causes RX interrupt in the Interrupt request and Polling modes.

When the transmitter transfers data from its transmit FIFO register to transmit shifter and the amount of data left in transmit FIFO is less than or equal to the TX FIFO trigger level, TX interrupt is generated (provided Transmit mode in control register is selected as Interrupt request or Polling mode). In non-FIFO mode, transferring the data from transmit holding register to transmit shifter generates TX interrupt in the Interrupt request and Polling mode.

The TX interrupt is always requested when the amount of data in the transmit FIFO is less than the trigger level. This indicates that an interrupt is requested when you enable the TX interrupt, unless you fill the TX buffer. Therefore, it is recommended to fill the TX buffer first and then enable the TX interrupt.

The interrupt controllers are categorized as the level-triggered type. You must set the interrupt type as Level when you program the UART control registers.

In this situation, when Receive and Transmit modes in control register are selected as DMAn request mode, the DMAn request occurs instead of RX or TX interrupt.

In DMA mode, size of transfer data is greater than FIFO size. After the data is completely transferred, DMA done occurs in DMAC. Then, change TX mode to INT/Polling mode so that TX REQ is not triggered.

Table 4-4 describes the interrupts in connection with FIFO.

Table 4-4 Interrupts in Connection with FIFO

Type	FIFO Mode	Non-FIFO Mode
RX interrupt	Generated when RX FIFO count is greater than or equal to the trigger level of received FIFO. Generated when the amount of data in FIFO does not reach RX FIFO trigger level and does not receive any data during the time specified (receive time out) in UCON.	Generated by receive holding register whenever receive buffer becomes full.
TX interrupt	Generated when TX FIFO count is less than or equal to the trigger level of transmit FIFO (TX FIFO trigger Level).	Generated by transmit holding register whenever transmit buffer becomes empty.
Error interrupt	Generated when Frame Error, Parity Error, or Break Signal are detected. Generated if UART receives new data when RX FIFO is full (overrun error).	Generated by all errors. However, when another error occurs at the same time, only one interrupt is generated.

4.2.8.1.5 UART Error Status FIFO

UART contains the error status FIFO besides the RX FIFO register. The Error Status FIFO indicates the date that is received with an error, among FIFO registers. An error interrupt is issued only when the data that contains error is ready to read out. To clear the error status FIFO, URXHn with an error and UERSTATn must be read out.

For example, it is assumed that the UART RX FIFO receives A, B, C, D, and E characters sequentially, and the Frame Error occurs when receiving B and the Parity Error occurs when receiving D.

The actual UART receive error does not generate any error interrupt, because the character, which was received with an error was not read. The error interrupt occurs when the character is read out.

Table 4-5 describes the Error interrupt.

Table 4-5 Error Interrupt

Time	Sequence Flow	Error Interrupt	Note
#0	When no character is read out	–	–
#1	A, B, C, D, and E is received	–	–
#2	After A is read out	Frame error (in B) interrupt occurs	The B has to be read out
#3	After B is read out	–	–
#4	After C is read out	Parity error (in D) interrupt occurs	The "D has to be read out
#5	After D is read out	–	–
#6	After E is read out	–	–

Figure 4-19 illustrates the UART Error Status FIFO.

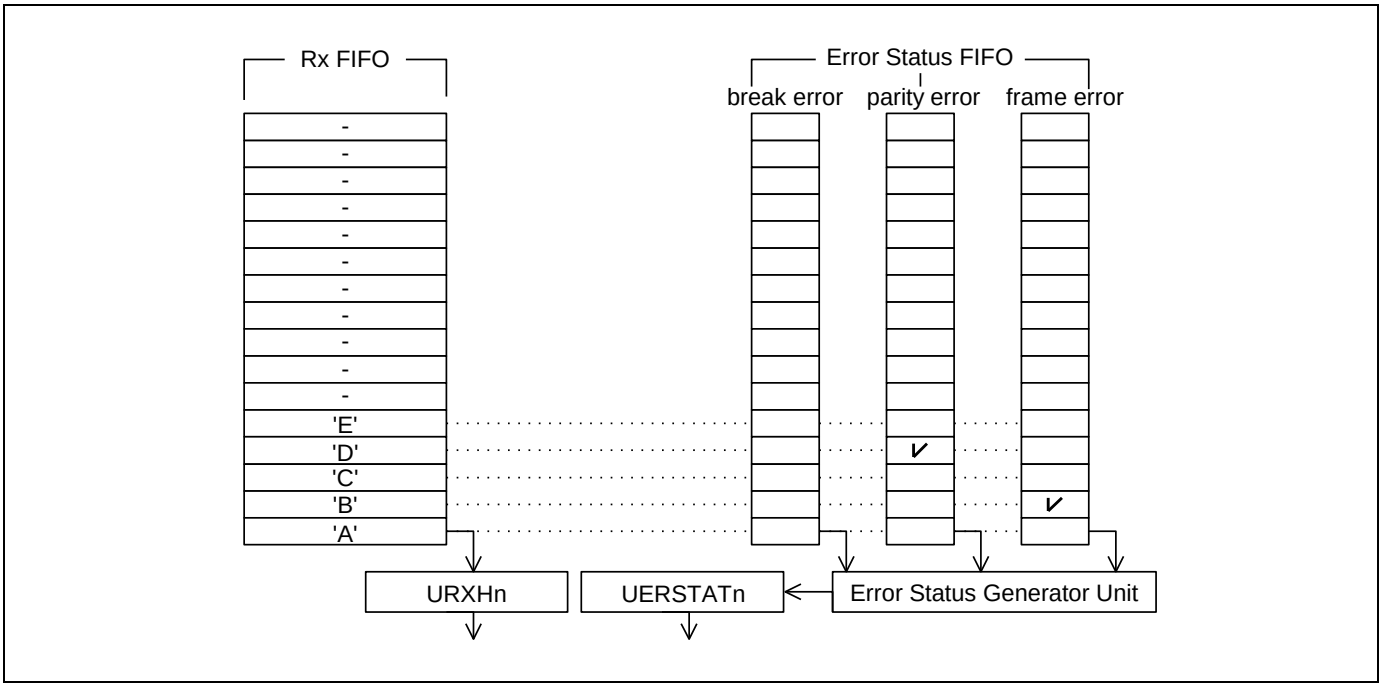


Figure 4-19 UART Receives the Five Characters Including Two Errors

4.2.8.2 Register Description

This section describes the register map information and its associated registers.

4.2.8.2.1 Register Map Summary

- Base Address: 0x4000_A000

Register	Offset	Description	Reset Value
ULCON	0x0000	Line Control.	0x0000_0000
UCON	0x0004	Control	0x0000_3000
UFCON	0x0008	FIFO Control	0x0000_0000
UMCON	0x000C	AFC Control	0x0000_0000
UTRSTAT	0x0010	TX/RX status	0x0000_0002
UERSTAT	0x0014	RX Error Status	0x0000_0000
UFSTAT	0x0018	FIFO Status	0x0000_0000
RSVD	0x001C	Reserved	0x0000_0000
UTXH	0x0020	Transmit Data for UART	0x0000_0000
URXH	0x0024	Receive Data for UART	0x0000_0000

Register	Offset	Description	Reset Value
UBRDIV	0x0028	Baud Rate Division Value	0x0000_0000
UFRACVAL	0x002C	Fractional part of Baud Rate Divisor	0x0000_0000
UINTP	0x0030	Interrupt Pending	0x0000_0000
UINTS	0x0034	Interrupt Source	0x0000_0000
UINTM	0x0038	Interrupt Mask	0x0000_0000

NOTE: If reserved or empty addresses in the register map are changed, S1SBP6A cannot guarantee normal operation.

4.2.8.2.1.1 ULCON

- Base Address: 0x4000_A000
- Address = Base Address + 0x0000, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD0	[31:6]	RW	Reserved	0x0000_0000
Parity_mode	[5:3]	RW	Specifies the type of parity generation to be performed and checked during UART transmit and receive operation. 0xx: No parity 100: Odd parity 101: Even parity 110: Parity forced/ checked as 1 111: Parity forced/ checked as 0	0x0000_0000
Number_of_stop_bit	[2]	RW	Specifies the number of stop bits that are used to signal end-of-frame signal. 0 = One stop bit per frame 1 = Two stop bit per frame	0x0000_0000
Word_length	[1:0]	RW	Indicates the number of data bits to be transmitted or received per frame. 00: 5-bit 01: 6-bit 10: 7-bit 11: 8-bit	0x0000_0000

4.2.8.2.1.2 UCON

- Base Address: 0x4000_A000
- Address = Base Address + 0x0004, Reset Value = 0x0000_3000

Name	Bit	Type	Description	Reset Value
RSVD0	[31:23]	RW	Reserved	0x0000_0000
Tx_DMA_burst_size	[22:20]	RW	* TX DMA Burst Size Indicates the data transfer size of one DMA transaction which is triggered by a TX DMA request. The DMA program must be programmed to transfer the same data size as this value for a single TX DMA request. 000: 1 byte (Single) 001: 4 bytes 010: 8 bytes 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved	0x0000_0000
RSVD1	[19]	RW	Reserved	0x0000_0000
Rx_DMA_burst_size	[18:16]	RW	* RX DMA Burst Size Indicates the data transfer size of one DMA transaction that is triggered by a RX DMA request. The DMA program must be programmed to transfer the same data size as this value for a single RX DMA request: 000: 1 byte (Single) 001: 4 bytes 010: 8 bytes 011: 16 bytes 100: Reserved 101: Reserved 110: Reserved 111: Reserved	0x0000_0000
Rx_timeout_interrupt_interval	[15:12]	RW	RX Timeout Interrupt Interval RX interrupt occurs when no data is received during 8 X (N+1) frame time. The default value of this field is 3 and it indicates the timeout interval is 32 frame time.	0x0000_0003
Rx_Time_out_with_empty_Rx_FIFO	[11]	RW	* Enables RX time-out feature when RX FIFO counter is 0 This bit is valid only when UCONn[7] is 1: 0: Disables RX time-out feature when RX FIFO is empty 1: Enables RX time-out feature when RX FIFO is empty	0x0000_0000
Rx_Time_out_DMA_suspend_enable	[10]	RW	* Enables RX DMA FSM to suspend when RX Time-out occurs 0: Disables suspending RX DMA FSM 1: Enables suspending RX DMA FSM	0x0000_0000

Name	Bit	Type	Description	Reset Value
Tx_Interrupt_Type	[9]	RW	* Interrupt request type 0: Pulse (interrupt is requested when the TX buffer is empty in the non-FIFO mode or when it reaches TX FIFO trigger level in the FIFO mode) 1: Level (interrupt is requested when TX buffer is empty in the non-FIFO mode or when it reaches TX FIFO trigger level in the FIFO mode)	0x0000_0000
Rx_Interrupt_Type	[8]	RW	* Interrupt request type 0: Pulse (interrupt is requested when instant RX buffer receives data in the non-FIFO mode or when it reaches RX FIFO trigger level in the FIFO mode) 1: Level (interrupt is requested when RX buffer receives data in the non-FIFO mode or when it reaches RX FIFO trigger level in the FIFO mode)	0x0000_0000
Rx_Time_Out_Enable	[7]	RW	* Enables/Disables RX time-out interrupts when UART FIFO is enabled. The interrupt is a receive interrupt. 0: Disables RX time-out interrupt 1: Enables RX time-out interrupt	0x0000_0000
Rx_Error_Status_Interrupt_Enable	[6]	RW	* Enables the UART to generate an interrupt upon an exception(Break, Frame Error, Parity Error, or Overrun Error during a receive operation) 0: Does not generate receive error status interrupt 1: Generates receive error status interrupt	0x0000_0000
Loop_back_Mode	[5]	RW	* Setting loop-back bit to 1 triggers the UART to enter the loop-back mode. This mode is provided for test only. 0: Normal operation 1: Loop-back mode	0x0000_0000
Send_Break_Signal	[4]	RW	* Setting this bit triggers the UART to send a break during 1 frame time. This bit is automatically cleared after sending the break signal. 0: Normal transmit 1: Sends the break signal	0x0000_0000
Transmit_Mode	[3:2]	RW	* Determines which function is able to write TX data to the UART transmit buffer. 00: Disables 01: Interrupt request or Polling mode 10: DMA mode 11: Reserved	0x0000_0000
Receive_Mode	[1:0]	RW	* Determines which function is able to read data from UART receive buffer. 00: Disables 01: Interrupt request or Polling mode 10: DMA mode 11: Reserved	0x0000_0000

NOTE:

1. DIV_VAL = UBRDIV + UFRACVAL/16. For more information, refer to UBRDIV and UFRACVAL.
2. S1SBP6A uses a level-triggered interrupt controller. Therefore, these bits must be set to 1 for every transfer.
3. When the UART does not reach the FIFO trigger level and it does not receive data during the time specified at the RX Timeout Interrupt Interval field in DMA receive mode with FIFO, the RX interrupt is generated (receive time out). You must check the FIFO status and read out the rest.
4. UCON[11] and UCON[7] should be set to 1 to enable RX time-out feature when RX FIFO counter is 0.

4.2.8.2.1.3 UFCON

- Base Address: 0x4000_A000
- Address = Base Address + 0x0008, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD0	[31:11]	RW	Reserved	0x0000_0000
Tx_FIFO_Trigger_Level	[10:8]	RW	* Determines the trigger level of TX FIFO. When data count of TX FIFO is less than or equal to the trigger level TX interrupt occurs. 000: 0 byte 001: 8 bytes 010: 16 bytes 011: 24 bytes 100: 32 bytes 101: 40 bytes 110: 48 bytes 111: 56 bytes	0x0000_0000
RSVD1	[7]	RW	Reserved	0x0000_0000
Rx_FIFO_Trigger_Level	[6:4]	RW	* Determines the trigger level of RX FIFO. When data count of RX FIFO is greater than or equal to the trigger level RX interrupt occurs. 000: 8 byte 001: 16 bytes 010: 24 bytes 011: 32 bytes 100: 40 bytes 101: 48 bytes 110: 56 bytes 111: 64 bytes	0x0000_0000
RSVD2	[3]	RW	Reserved	0x0000_0000
Tx_FIFO_Reset	[2]	RW	* Auto-clears after resetting FIFO 0: Normal 1: TX FIFO reset	0x0000_0000
Rx_FIFO_Reset	[1]	RW	* Auto-clears after resetting FIFO 0: Normal 1: RX FIFO reset	0x0000_0000

Name	Bit	Type	Description	Reset Value
FIFO_Enable	[0]	RW	* FIFO Enable 0: Disables 1: Enables	0x0000_0000

NOTE: When the UART does not reach the FIFO trigger level and does not receive data during the specified timeout interval in DMA receive mode with FIFO, the RX interrupt is generated (receive time out). You must check the FIFO status and read out the rest.

4.2.8.2.1.4 UMCON

- Base Address: 0x4000_A000
- Address = Base Address + 0x000C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RTS_trigger_level	[7:5]	RW	* Determines the trigger level of RX FIFO to control nRTS signal. When AFC bit is enabled and RX FIFO have bytes that are greater than or equal to the trigger level, nRTS signal is deactivated. 000: 63 bytes 001: 56 bytes 010: 48 bytes 011: 40 bytes 100: 32 bytes 101: 24 bytes 110: 16 bytes 111: 8 bytes	0x0000_0000
AFC	[4]	RW	* Auto flow control 0: Disables 1: Enables	0x0000_0000
RSVD0	[3:1]	RW	These bits must be 0.	0x0000_0000
Request_to_send	[0]	RW	* When AFC bit is enabled, this value is ignored. In this case. it automatically controls nRTS signals. When AFC bit is disabled, the software must control nRTS signal. 0: H level (Inactivate nRTS) 1: L level (Activate nRTS)	0x0000_0000

NOTE: In AFC mode, RX FIFO trigger level should be set to lesser than RTS trigger level, because transmitter stops data transfer when it receives deactivated nRTS signal.

4.2.8.2.1.5 UTRSTAT

- Base Address: 0x4000_A000
- Address = Base Address + 0x0010, Reset Value = 0x0000_0002

Name	Bit	Type	Description	Reset Value
Rx_FIFO_count_in_Rx_time_out_status	[23:16]	R	RX FIFO counter capture value when RX time-out occurs	0x0000_0000
Tx_DMA_FSM_state	[15:12]	R	* Current State of TX DMA FSM 0x0: Idle 0x1: Burst Request 0x2: Burst Acknowledgement 0x3: Burst Next (intermediate state for next request) 0x4: Single Request 0x5: Single Acknowledgement 0x6: Single Next (intermediate state for next request) 0x7: Reserved 0x8: Reserved 0x9: Reserved 0x10: Reserved	0x0000_0000
Rx_DMA_FSM_state	[11:8]	R	* Current State of RX DMA FSM 0x0: Idle 0x1: Burst Request 0x2: Burst Acknowledgement 0x3: Burst Next (intermediate state for next request) 0x4: Single Request 0x5: Single Acknowledgement 0x6: Single Next (intermediate state for next request) 0x7: Reserved 0x8: Reserved 0x9: Reserved 0x10: Reserved	0x0000_0000
RSVD0	[7:4]	R	Reserved	0x0000_0000
Rx_time_out_status_clear	[3]	RW	* RX Time-out status when read 0: RX Time-out did not occur 1: RX Time-out occurs * Clear RX Time-out status when write 0: No operation 1: Clears RX Time-out status *NOTE: If UCONn[10] is set to 1, writing 1 to this bit resumes RX DMA FSM that was suspended when RX time-out had occurred.	0x0000_0000
Transmitter_empty	[2]	R	* This bit is automatically set to 1 when the transmit buffer has no valid data to transmit and the transmit shift is empty. 0: Buffer is not empty	0x0000_0000

Name	Bit	Type	Description	Reset Value
			1: Transmitter (that includes transmit buffer and shifter) empty	
Transmit_buffer_empty	[1]	R	* This bit is automatically set to 1 when transmit buffer is empty 0: Buffer is not empty 1: Buffer is empty In non-FIFO mode, interrupt or DMA is requested. In FIFO mode, Interrupt or DMA is requested when TX FIFO trigger level is set to 00 (empty). When UART uses FIFO, check TX FIFO count bits and TX FIFO full bit in UFSTAT instead of this bit.	0x0000_0001
Receive_buffer_data_ready	[0]	R	* This bit is automatically set to 1 if receive buffer contains valid data which is received through the RXDn port 0: Buffer is empty 1: Buffer has a received data (In non-FIFO mode, Interrupt or DMA is requested). When UART uses the FIFO, check RX FIFO count bits and RX FIFO full bit in UFSTAT instead of this bit.	0x0000_0000

4.2.8.2.1.6 UERSTAT

- Base Address: 0x4000_A000
- Address = Base Address + 0x0014, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
Break_detect	[3]	R	* This bit is automatically set to 1 to indicate that a break signal has been received. 0: No break signal is received 1: Break signal is received (Interrupt is requested)	0x0000_0000
Frame_error	[2]	R	* This bit is automatically set to 1 when a Frame Error occurs during the receive operation. 0: No Frame Error occurs during the receive operation 1: Frame Error occurs (interrupt is requested) during the receive operation	0x0000_0000
Parity_error	[1]	R	* This bit is automatically set to 1 when a Parity Error occurs during the receive operation. 0: No Parity Error occurs during receive operation 1: Parity Error occurs (interrupt is requested) during the receive operation	0x0000_0000
Overrun_error	[0]	R	* This bit is automatically set to 1 automatically when an Overrun Error occurs during the receive operation. 0: No Overrun Error occurs during the receive operation 1: Overrun Error occurs (interrupt is requested) during the receive operation	0x0000_0000

NOTE: These bits (UERSAT[3:0]) are automatically cleared to 0 when UART error status is read.

4.2.8.2.1.7 UFSTAT

- Base Address: 0x4000_A000
- Address = Base Address + 0x0018, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
Tx_FIFO_full	[24]	R	* This bit is automatically set to 1 when the transmitted FIFO is full during transmit operation 0: Not Full 1: Full	0x0000_0000
Tx_FIFO_count	[23:16]	R	Number of data in TX FIFO * Note: This field is set to 0 when TX FIFO is full.	0x0000_0000
RSVD0	[15:10]	R	Reserved	0x0000_0000
Rx_FIFO_error	[9]	R	This bit is set to 1 when RX FIFO contains invalid data which results due to Frame Error, Parity Error, or Break Signal.	0x0000_0000
Rx_FIFO_full	[8]	R	* This bit is automatically set to 1 when the received FIFO is full during receive operation 0: Not Full 1: Full	0x0000_0000
Rx_FIFO_count	[7:0]	R	Number of data in RX FIFO * Note: This field is set to 0 when RX FIFO is full.	0x0000_0000

4.2.8.2.1.8 RSVD

- Base Address: 0x4000_A000
- Address = Base Address + 0x001C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD0	[31:0]	R	Reserved	0x0000_0000

4.2.8.2.1.9 UTXH

- Base Address: 0x4000_A000
- Address = Base Address + 0x0020, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
UTXH	[7:0]	W	Transmit Data for UART	0x0000_0000

4.2.8.2.1.10 URXH

- Base Address: 0x4000_A000
- Address = Base Address + 0x0024, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
URXH	[7:0]	R	Receive Data for UART	0x0000_0000

NOTE: When an Overrun Error occurs, the URXH must be read. If not, the next received data generates an Overrun Error, even though the overrun bit of UERSTAT had been cleared.

4.2.8.2.1.11 UBRDIV

- Base Address: 0x4000_A000
- Address = Base Address + 0x0028, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
UBRDIV	[15:0]	RW	Baud Rate Division Value * Note: UBRDIV value must be greater than 0.	0x0000_0000

4.2.8.2.1.12 UFRACVAL

- Base Address: 0x4000_A000
- Address = Base Address + 0x002C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
UFRACVAL	[3:0]	RW	Determines the fractional part of Baud Rate Divisor	0x0000_0000

NOTE:

1. UART Baud Rate Configuration

   The value stored in the Baud Rate Divisor (UBRDIV) and Divisor Fractional value (UFRACVAL) is used to determine the serial TX/RX clock rate (baud rate) as:

   DIV_VAL = UBRDIV + UFRACVAL/16

   Or

   DIV_VAL = (SCLK_UART/(bps × 16)) – 1

   Where, the divisor should be from 1 to (2^{16} – 1).

   Using UFRACVAL, you can generate the Baud Rate more accurately.

   For example, when the Baud Rate is 115200 bps and SCLK_UART is 40 MHz, UBRDIV and UFRACVAL are calculated using the following formula:

   DIV_VAL = (40000000/(115200 × 16)) – 1
   = 21.7 – 1
   = 20.7

   UBRDIV = 20 (integer part of DIV_VAL)

   UFRACVAL/16 = 0.7

   So, UFRACVAL = 11

2. Baud Rate Error Tolerance

   UART Frame error should be less than 3.12 % (5/160, with 1 Frame = 10 bit)

   tUPCLK = (UBRDIV + 1 + UFRACVAL/16) × 16 × 1Frame/SCLK_UART

   tUPCLK: Real UART Clock

tEXTUARTCLK = 1Frame/baud-rate
tEXTUARTCLK: Ideal UART Clock
UART error = (tUPCLK – tEXTUARTCLK)/tEXTUARTCLK × 100 %
* 1Frame = start bit + data bit + parity bit + stop bit.

3. UART Clock and PCLK Relation

There is a constraint on the ratio of clock frequencies for PCLK to UARTCLK.

The frequency of UARTCLK must not be more than 5.5/3 times faster than the frequency of PCLK:

FUARTCLK ⇐ 5.5/3 × FPCLK
FUARTCLK = baudrate × 16

This allows sufficient time to write the received data to the receive FIFO.

4.2.8.2.1.13 UINTP

- Base Address: 0x4000_A000
- Address = Base Address + 0x0030, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD0	[3]	RW	Reserved	0x0000_0000
TXD	[2]	RW	Generates Transmit interrupt	0x0000_0000
ERROR	[1]	RW	Generates Error interrupt	0x0000_0000
RXD	[0]	RW	Generates Receive interrupt	0x0000_0000

NOTE:
1. Interrupt pending contains information of the interrupts that are generated.
2. If one of these 3 bits is logical high (1), each UART channel generates interrupt.
3. This must be cleared in the interrupt service routine after clearing the interrupt pending in Interrupt Controller (INTC). Clear specific bits of UINTP by writing 1 to the bits that you want to clear.

4.2.8.2.1.14 UINTS

- Base Address: 0x4000_A000
- Address = Base Address + 0x0034, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD0	[3]	R	Reserved	0x0000_0000
TXD	[2]	R	Generates Transmit interrupt	0x0000_0000
ERROR	[1]	R	Generates Error interrupt	0x0000_0000
RXD	[0]	R	Generates Receive interrupt	0x0000_0000

NOTE: Interrupt Source contains information of the interrupt that are generated, regardless of the value of Interrupt Mask

4.2.8.2.1.15 UINTM

- Base Address: 0x4000_A000
- Address = Base Address + 0x0038, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD0	[3]	RW	Reserved	0x0000_0000
TXD	[2]	RW	Mask Transmit interrupt	0x0000_0000
ERROR	[1]	RW	Mask Error interrupt	0x0000_0000
RXD	[0]	RW	Mask Receive interrupt	0x0000_0000

Figure 4-20 illustrates the block diagram of UNITS, UINTP and UINTM.

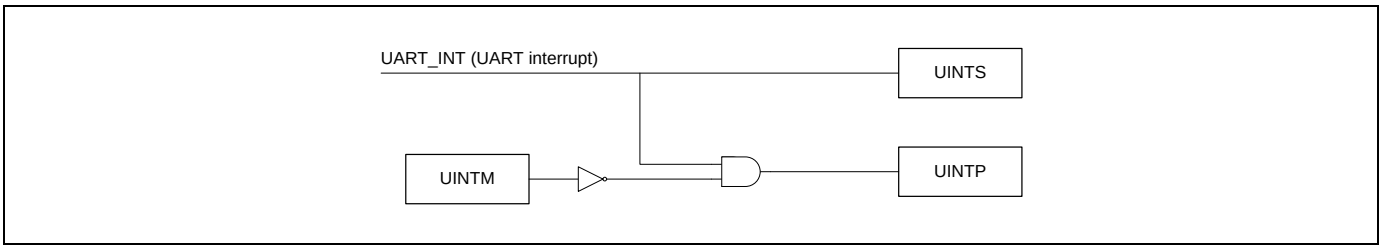


Figure 4-20 Block Diagram of UINTS, UINTP and UINTM

NOTE:

1. Interrupt Mask contains information about the interrupt source that is masked. When a specific bit is set to 1, interrupt request signal to the Interrupt Controller is not generated even though corresponding Interrupt Source is generated.
2. If the Mask bit is 0, the interrupt requests are serviced from the corresponding Interrupt Source.

4.2.9 Inter-Integrated Circuit

Inter-Integrated Circuit (I2C) unit supports serial data communication with the following features:

- DMA-based or interrupt-based operation
- Separate transmission and reception of data
- Non-integer clock division
- Master and slave operation modes

Figure 4-21 illustrates a block diagram of HSI2C

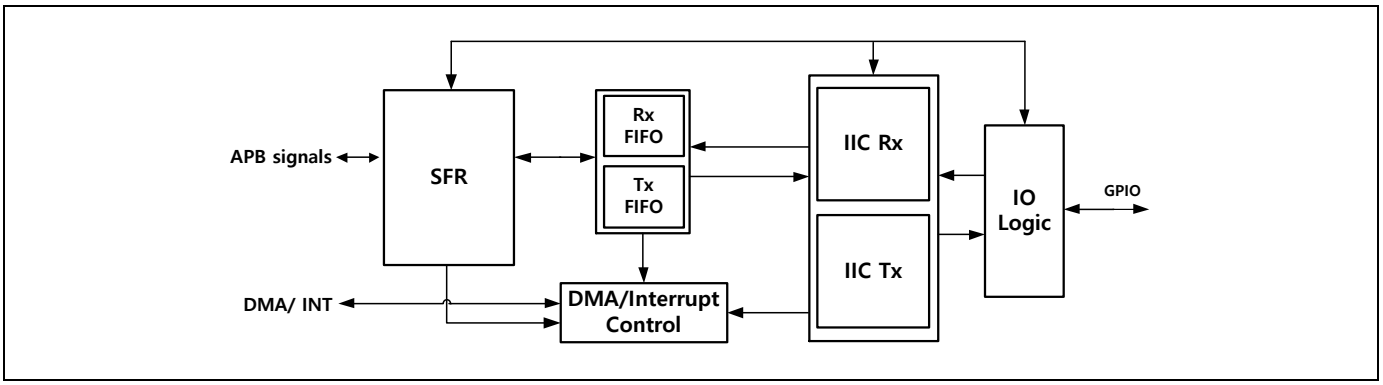


Figure 4-21 Block Diagram of HSI2C

4.2.9.1 Functional Description

The HSI2C unit supports Interrupt/DMA operation, master / slave mode, and two channels, such as HSI2C TX and HSI2C RX channels.

To write data in TX FIFO, the MCU (or DMA) must write data in TXDATA register. The data is automatically moved to TX FIFO.

To read data from RX FIFO, the MCU (or DMA) must access the RXDATA register and data is automatically sent to RXFIFO register.

4.2.9.1.1 FIFO Access

The HSI2C unit supports access to FIFOs. The data size is selected from 8-bit, 16-bit, or 32-bit data. The trigger level of each FIFO is set from 0 byte to 16 byte. The channel (TX or RX) accesses FIFO using 8-bit data. FIFO is 8 bit wide and 16 depth.

4.2.9.1.2 Trailing Bytes

If the number of samples in RX FIFO is less than the threshold value and no additional data is received for a long time, the remaining bytes in RX FIFO is called as trailing bytes. To remove these bytes, the internal timer and interrupt signal are used. If internal timer value is zero, interrupt signal is generated and the CPU can remove the trailing bytes.

4.2.9.1.3 Start and Stop Conditions

The master device generates Start and Stop conditions. After initiating Start condition, the master writes the 7-bit slave address in the first outgoing data byte to select the slave device. The 8th bit determines the direction of transfer (read or write). The I2C-bus gets busy if a Start condition is generated and a Stop condition frees the I2C-bus.

Each data byte put onto the SDA line must be of eight bits. There is no limit to send or receive bytes during the bus transfer operation. Data is always sent first from MSB and every byte must be followed by acknowledge (ACK) bit. *Figure 4-22* illustrates Start and Stop Conditions.

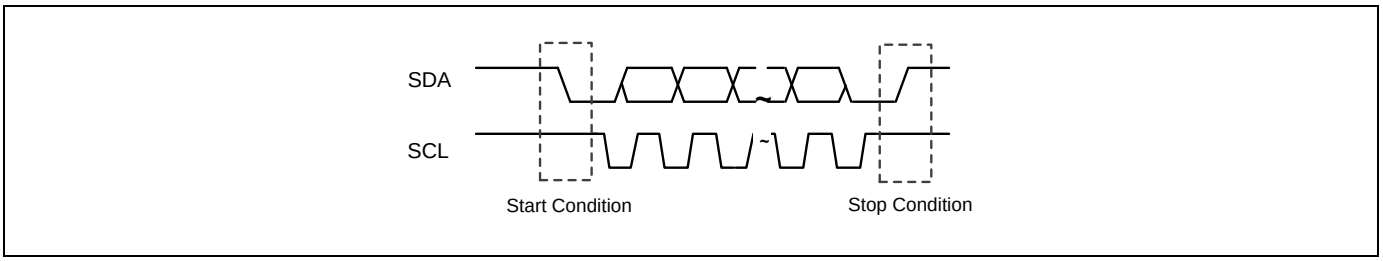


Figure 4-22 Start and Stop Conditions

4.2.9.1.4 ACK Signal Transmission

To complete a one-byte transfer operation, the receiver must send an ACK bit to the transmitter. The ACK pulse occurs at the ninth clock of the SCL line. Eight clocks are required for the one-byte data transfer. The master generates clock pulse required to transmit the ACK bit.

The transmitter releases the SDA line by making the SDA line High if the ACK clock pulse is received. The receiver drives the SDA line Low during the ACK clock pulse, so that the SDA keeps Low during the High period of the ninth SCL pulse.

The software (CTL) enables or disables ACK bit transmit function. However, the ACK pulse on the ninth clock of SCL is required to complete the one-byte data transfer operation. *Figure 4-23* illustrates Acknowledge on I2C-bus Block Diagram

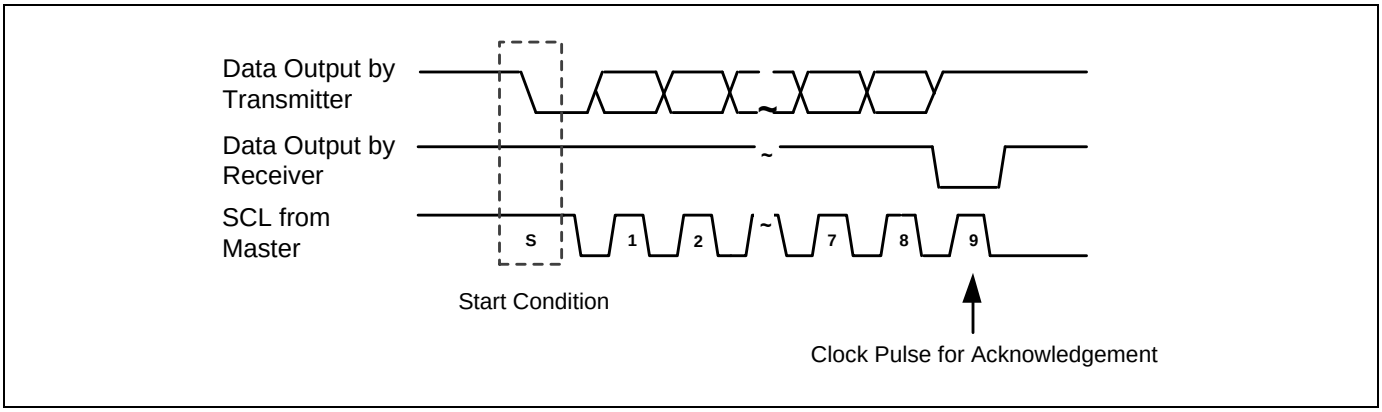


Figure 4-23 Acknowledge on I2C-bus Block Diagram

4.2.9.1.5 Bus Arbitration Procedures

Arbitration takes place on the SDA line to prevent the contention on the bus between two masters. If a master with SDA High level detects other master with SDA active Low level, it does not initiate a data transfer because the current level on the bus does not correspond to its own. The arbitration procedure is extended until the SDA line turns High.

If the masters lower the SDA line simultaneously, each master evaluates whether the mastership is allocated itself or not. For the purpose of evaluation, each master detects the address bits. When each master generates the slave address, it detects the address bit on the SDA line because the SDA line is likely to get Low rather than to keep High.

Assume that one master generates a Low as first address bit, while the other master is maintaining High. In this case, both masters detect Low on the bus because the Low status has superior priority than the High status. If this happens, the master that generates a Low output (as the first bit of address) gets the mastership and the master that generates a High output (as the first bit of address) withdraws the mastership.

If both masters generate Low as the first bit of address, there is arbitration for the second address bit again. This arbitration continues to the end of last address bit.

Assume that both masters trying to address the same device, there will be arbitration again for the data-bits.

4.2.9.1.6 Abort Conditions

If a slave receiver cannot acknowledge the confirmation of the slave address, it holds the level of the SDA line High. In this case, the master generates a Stop condition to abort the transfer.

If a master receiver aborts the transfer, it signals the end of the slave transmit operation by canceling the generation of an ACK after the last data byte received from the slave. The slave transmitter releases the SDA to allow a master to generate a Stop condition.

4.2.9.1.7 Fast-Speed Mode

Each byte placed on the SDA line must be eight bits in length. There is no limit to the number of bytes transmitted per transfer. The first byte following a Start condition has the address field. The address field can be transmitted by the master when the I2C-bus is operating in Master mode. Each byte is followed by an acknowledgement (ACK) bit. The MSB bit of the serial data and addresses are always sent first.

Figure 4-24 illustrates data transfer format in fast-speed mode.

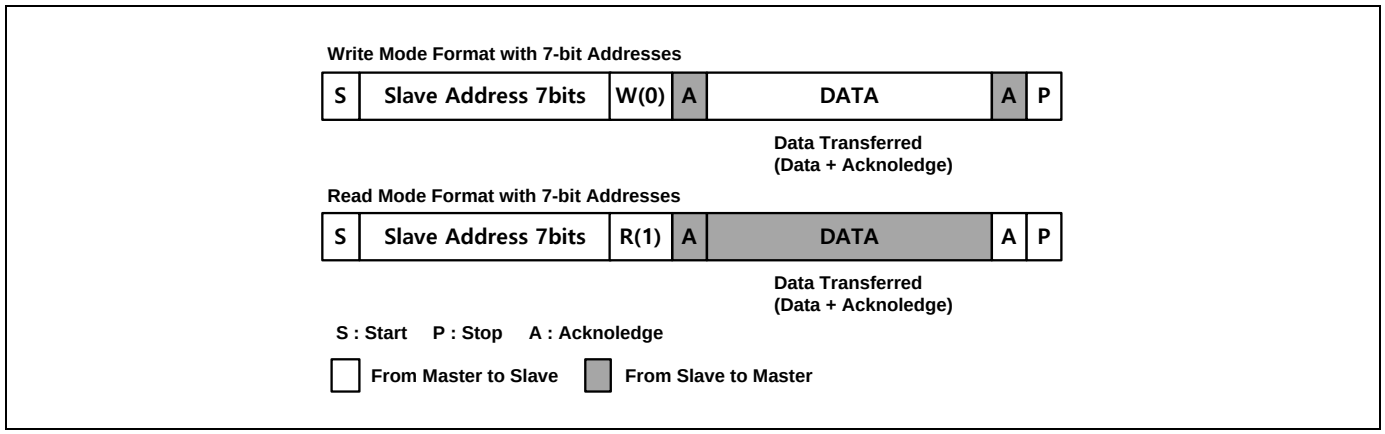


Figure 4-24 Data Transfer Format in Fast-Speed Mode

4.2.9.1.8 High-Speed Mode

Serial data transfer format in high-speed mode meets the standard-mode (fast-speed mode) I2C-bus specification. High-speed mode can only commence after the following conditions are satisfied (all of which are in fast-speed mode):

1. START condition (S)
2. 8-bit master id code (00001xxx)
3. Non-acknowledge bit

High-speed master id codes are reserved 8-bit codes, which are not used for slave addressing or other purpose. *Figure 4-25* illustrates the data transfer format in high-speed mode.

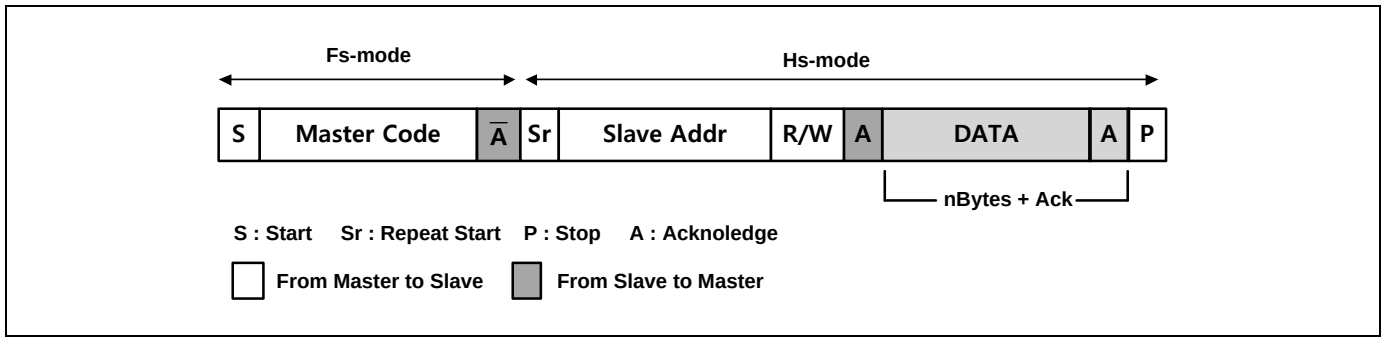


Figure 4-25 Data Transfer Format in High-Speed Mode

4.2.9.1.9 10-bit Slave-address Mode

I2C channel of HSI2C supports 10-bit slave-address mode and *Figure 4-26* and *Figure 4-27* illustrate data-transfer using 10-bit address.

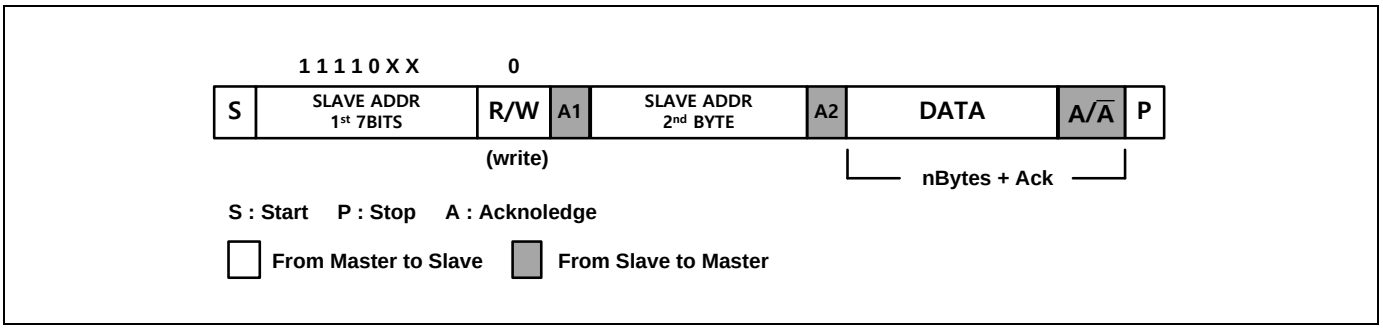


Figure 4-26 Master Transmitter Addresses Slave Receiver with 10-bit Address

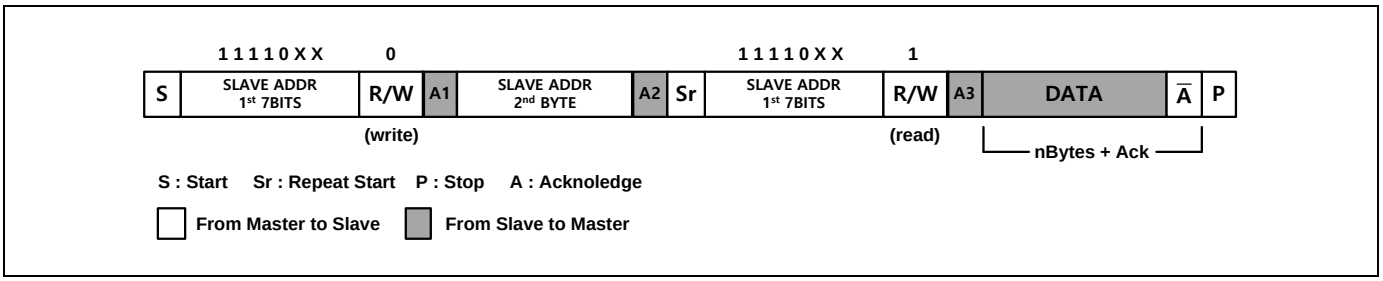


Figure 4-27 Master Receiver Addresses Slave Transmitter with 10-bit Address

4.2.9.1.10 Done Interrupt Recommendations

For auto mode and manual mode, there are several done interrupt signals like INT_TRANSFER_DONE_AUTO, INT_TRANS_ABORT_AUTO, INT_TRANSFER_DONE_MANUAL, and INT_TRANSFER_DONE_NOACK in the INT_STAT register. Exercise caution for the SCL clock stretching to use these interrupt signals in master operation mode. Some I2C slave device might use the SCL clock stretching to do something internally so that I2C slave device may hold the SCL line to Low.

General I2C slave does not use the SCL clock stretching. As illustrated in both *Figure 4-28* and *Figure 4-29*, they have a time interval difference. To check the final completion of the transfers, HSI2C master should check the master state if using the SCL clock stretching slaves. After detecting more than three interrupts, HSI2C master might check whether I2C_TRANS_STATUS[3:0](MASTER_ST) is 0 (IDLE) or I2C_TRANS_STATUS[17](MASTER_BUSY) is 0. If there is any SCL clock stretching by slave, both bit fields don't show 0. But these bit checking may delay the next operations of HSI2C, it should be considered to use or not according to the slave specification.

Note that this HSI2C also can stretch SCL Low in slave operation mode. For more information, refer to the I2C_CONF[9:8] (STRCH_MANUAL,STRCH_EN) bits.

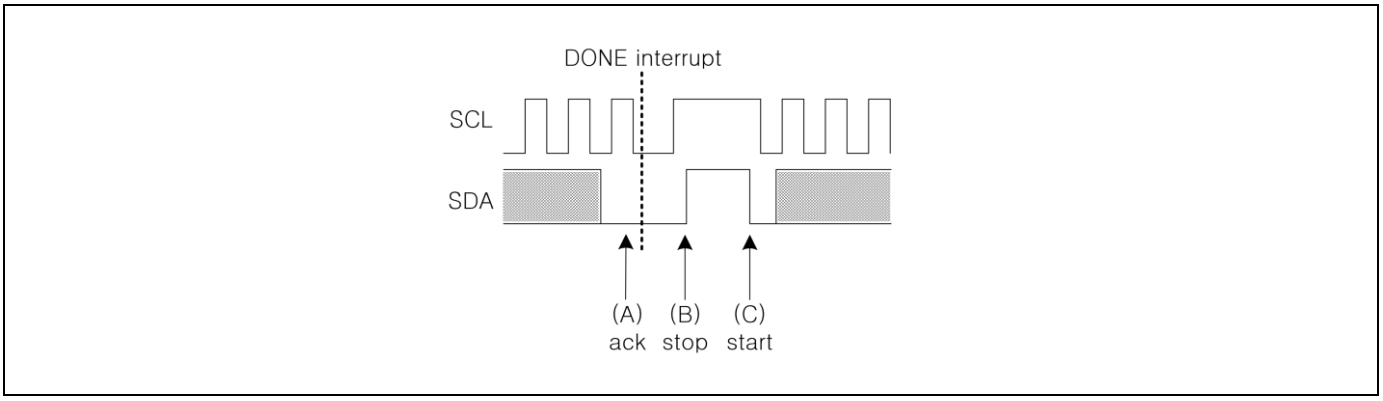


Figure 4-28 Done Interrupt Timing when Accessing General I2C Slaves

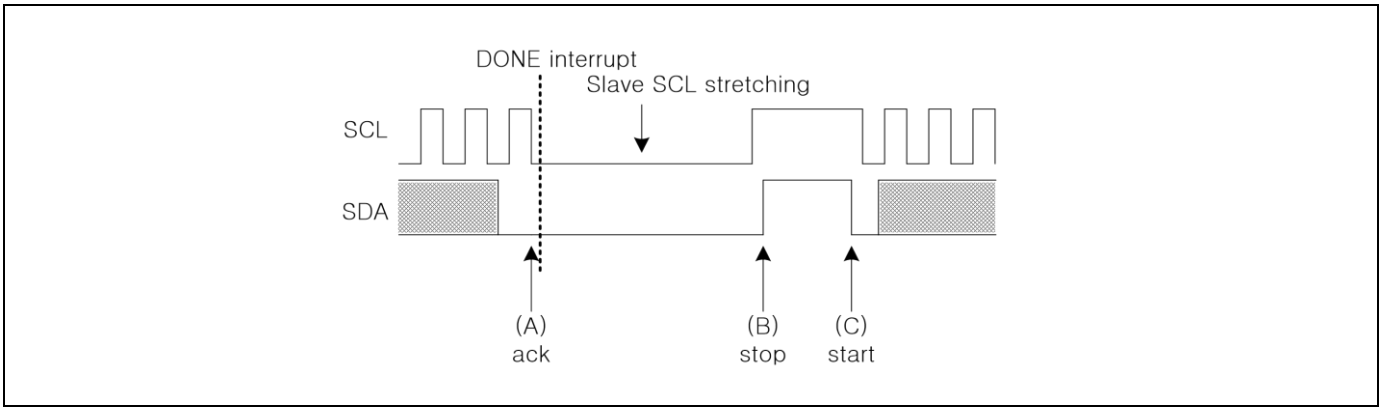


Figure 4-29 Done Interrupt Timing when Accessing SCL Clock Stretching I2C Slave

4.2.9.1.11 HSI2C Frequency Control

Register of HSI2C master controls the HSI2C clock (SCL) frequency using the following equation.

Clock generation equation of HSI2C clock frequency:

$$Fpclk/Fi2c = (CLK\_DIV+1) \times (TSCL\_L+TSCL\_H+2) + \{ (FLT\_CYCLE\_SCL+3) - (FLT\_CYCLE\_SCL+3)\%(CLK\_DIV+1) \} \times 2$$

Fi2c is the clock frequency of I2C channel.

Fpclk is the clock frequency of PCLK.

CLK_DIV is a bit field of I2C_TIMING_HS3 (for high-speed mode) or I2C_TIMING_FS3 (for fast-speedmode) SRs.

TSCL_L and TSCL_H are bit fields of I2C_TIMING_HS2 (for high-speed mode) or I2C_TIMING_FS2 (for fast-mode) SFRs

FLT_CYCLE_SCL is a bit field of I2C_CONF SFR.

% is modulo operator which is the remainder after division.

4.2.9.2 Register Description

This section describes the register map information and its associated registers.

4.2.9.2.1 Register Map Summary

- Base Address: 0x4001_2000

Register	Offset	Description	Reset Value
CTL	0x0000	HSI2C Control Register	0x0000_0000
FIFO_CTL	0x0004	HSI2C FIFO Control Register	0x0008_0083
TRAILING_CTL	0x0008	Specifies the count value from writing the last data in RX FIFO to flush trailing bytes in FIFO. Note: The counter is based on PCLK.	0xFFFF_FFFF
INT_EN	0x0020	HSI2C Interrupt Enable Register	0x0000_0000
INT_STAT	0x0024	HSI2C Interrupt Register	0x0000_0000
FIFO_STAT	0x0030	HSI2C FIFO Status Register	0x0100_0100
TXDATA	0x0034	Transmit Data Buffer for HSI2C	0xDEAD_BEAF
RXDATA	0x0038	Received Data Buffer for HSI2C.	0x0000_0000
I2C_CONF	0x0040	I2C Configuration	0x9803_C1FF
I2C_AUTO_CONF	0x0044	I2C Configuration for AUTO Mode	0x0003_00FF
I2C_TIMEOUT	0x0048	Time Out for I2C Master	0x8000_00FF
I2C_MANUAL_CMD	0x004C	Command Register for MANUAL Mode	0x0000_0000
I2C_TRANS_STATUS	0x0050	HSI2C Transfer Status Register	0x0000_0000
I2C_TIMING_HS1	0x0054	Timing Parameter for High-Speed Mode	0x0F0F_0F00
I2C_TIMING_HS2	0x0058	Timing Parameter for High-Speed Mode	0x0F0F_FFFF
I2C_TIMING_HS3	0x005C	Timing Parameter for High-Speed Mode	0x00FF_00FF
I2C_TIMING_FS1	0x0060	Timing Parameter for Fast-Speed mode	0x0F0F_0F00
I2C_TIMING_FS2	0x0064	Timing Parameter for Fast-Speed Mode	0x0F0F_FFFF
I2C_TIMING_FS3	0x0068	Timing Parameter for Fast-Speed Mode	0x00FF_00FF
I2C_TIMING_SLA	0x006C	Data Hold Timing for I2C Slave. (data transition after SCL falling-edge) (For both auto and manual modes)	0x0000_00FF
I2C_ADDR	0x0070	*Address Register I2C Slave Address I2C Master ID Slave Address for Master	0xFF0F_FFFF

NOTE: If reserved or empty addresses in the register map are changed, S1SBP6A cannot guarantee normal operation.

4.2.9.2.1.1 CTL

- Base Address: 0x4001_2000
- Address = Base Address + 0x0000, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
SW_RST	[31]	W	Indicates software reset signal This bit clears the following registers and bits: Most writable registers with HSI2C_CTL(without [31] SW_RST), HSI2C_FIFO_CTL, HSI2C_TRAILING_CTL, HSI2C_INT_EN, I2C_CONF, I2C_AUTO_CONF, I2C_TIMEOUT, I2C_TIMING_HS1~3, I2C_TIMING_FS1~3, I2C_TIMING_SLA, I2C_ADDR 0 = Inactive software reset 1 = Active software reset	0x0000_0000
RSVD0	[30:29]	RW	Reserved	0x0000_0000
NO_ARB_FASTSDA	[28]	RW	Generally, this bit should be 0. This bit deactivates the modified logic of the abnormal operation problem when SCL is falling and then SDA is driven too quickly by other I2C device during 1 PCLK period. 0 = Don't check the arbitration during the first clock of SCL falling. 1 = Restore original logic	0x0000_0000
RSVD1	[27:20]	RW	Reserved	0x0000_0000
TX_BIT_SWAP	[19]	RW	Turn on or turn off bit swap operation on TX channel 0 = Off 1 = On	0x0000_0000
RSVD2	[18:17]	RW	Reserved	0x0000_0000
RX_BIT_SWAP	[16]	RW	Turn on or turn off bit swap operation on RX channel 0 = Off 1 = On	0x0000_0000
RSVD3	[15:14]	RW	Reserved	0x0000_0000
BUS_WIDTH	[13:12]	RW	00 = Byte 01 = Halfword 10 = Word 11 = Reserved	0x0000_0000
RSVD4	[11:10]	RW	Note = This bit should be set 00 for I2C.	0x0000_0000
RSVD5	[9:7]	RW	Reserved	0x0000_0000
RXCHON	[6]	RW	RX trailing count enable signal 0 = Disables 1 = Enables Note = Trailing byte INT works only when RXCHON is enabled	0x0000_0000

Name	Bit	Type	Description	Reset Value
			and INT_TRAILING_EN is enabled.	
TX_MODE	[5]	RW	Determines which function is used to read data from transmit buffer register 0 = Interrupt 1 = DMA	0x0000_0000
RX_MODE	[4]	RW	Determines which function is used to write data into receiver buffer register 0 = Interrupt 1 = DMA	0x0000_0000
MASTER	[3]	RW	Determines whether HSI2C is master or slave 0 = Slave 1 = Master	0x0000_0000
NO_1CYC_EDGE_SDA	[2]	RW	Generally, this bit should be 0. This bit deactivates the logic to restore internal SDA edge detect logic to 2 cycle latency instead of 1 cycle latency style. SDA 1 cycle latency edge detect logic is inserted to remove stop condition when SDA is rising 1 cycle after SCL rising. 0 = 1 cycle latency 1 = 2 cycle latency	0x0000_0000
NO_TSCL_H_0	[1]	RW	Generally, this bit should be 0. This bit deactivates the logic for the case of TSCL_H_FS=0 or TSCL_H_HS=0. 0 = Enable the case of TSCL_H_FS=0 or TSCL_H_HS=0. 1 = Deactivate this additional function.	0x0000_0000
CS_ENB	[0]	RW	Generally, this bit should be 0 (for both HS mode and FS mode). This bit deactivates current source pull-up function for SCL signal in HS mode. 0 = Enable current source for SCL signal to support high-speed operation 1 = Same driving for HS mode as FS mode	0x0000_0000

NOTE: Swap-operation:

Data for I2C function are transferred by SFR directly (the FIFO is not used).

Therefore, I2C function does not support swap-operation.

Swap-operation

Bit-swap:

Bit-swap operation is based on byte. For more information, refer the following example:

Data[31:0] → (bit-swap) {data[24], data[25], data[26], data[27], data[28],data[29], data[30], data[31], data[16], data[17], data[18], data[19], data[20], data[21], data[22], data[23], data[8], data[9], data[10], data[11], data[12], data[13], data[14], data[15], data[0], data[1], data[2], data[3], data[4], data[5], data[6], data[7]}

4.2.9.2.1.2 FIFO_CTL

- Base Address: 0x4001_2000
- Address = Base Address + 0x0004, Reset Value = 0x0008_0083

Name	Bit	Type	Description	Reset Value
Tx_FIFO_trigger_level	[22:16]	RW	Specifies the trigger level to generate TXFIFO_ALMOST_EMPTY interrupt (Note: NOT TXFIFO_UNDERRUN or TXFIFO_OVERRUN interrupts). If the byte number in TX FIFO is less than the trigger level, the TXFIFO_ALMOST_EMPTY interrupt is generated. * Note: The trigger level is used for both interrupt and DMA-request. The maximum value is 16.	0x0000_0008
RSVD0	[15:11]	RW	Reserved	0x0000_0000
Rx_FIFO_trigger_level	[10:4]	RW	Specifies the trigger level to generate RXFIFO_ALMOST_FULL interrupt (Note: NOT RXFIFO_UNDERRUN or RXFIFO_OVERRUN interrupts). If the byte number in RX FIFO is larger than the trigger level, the RXFIFO_ALMOST_FULL interrupt is generated. * Note: The trigger level is used for both interrupt and DMA-request. The maximum value is 16.	0x0000_0008
TX_FIFO_RST	[3]	RW	Reset TX FIFO	0x0000_0000
RX_FIFO_RST	[2]	RW	Reset RX FIFO	0x0000_0000
TXFIFO_EN	[1]	RW	* Specifies the TX FIFO enable signal 0: Disables (FIFO-depth = 1byte) 1: Enables (FIFO-depth = 16 bytes)	0x0000_0001
RXFIFO_EN	[0]	RW	* Specifies the RX FIFO enable signal 0: Disables (FIFO-depth = 1byte) 1: Enables (FIFO-depth = 16 bytes)	0x0000_0001

NOTE: FIFO_CTL is used for both INT mode and DMA mode

4.2.9.2.1.3 TRAILING_CTL

- Base Address: 0x4001_2000
- Address = Base Address + 0x0008, Reset Value = 0xFFFF_FFFF

Name	Bit	Type	Description	Reset Value
RSVD0	[31:24]	RW	Reserved	0x0000_00FF
TRAILING_CTL	[23:0]	RW	Specifies the count value from writing the last data in RX FIFO to flush trailing bytes in FIFO. * Note: The counter is based on PCLK.	0x00FF_FFFF

4.2.9.2.1.4 INT_EN

- Base Address: 0x4001_2000
- Address = Base Address + 0x0020, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
INT_SLAVE_ADDR_MATCH_EN	[15]	RW	* I2C slave address is matched (for slave mode only) 0: Disables 1: Enables	0x0000_0000
INT_LOSE_ARB_MANUAL_EN	[14]	RW	* Lost arbitration during executing command (for manual mode only) 0: Disables 1: Enables	0x0000_0000
INT_TRANSFER_DONE_MANUAL_EN	[13]	RW	* One byte (data or address) is transmitted successfully, one byte data is received successfully or command (start or stop) is completed. (for manual mode only) * Note: In high-speed mode, completion of master-ID-transfer does not assert this bit. 0: Disables 1: Enables	0x0000_0000
INT_TRANSFER_DONE_NOACK_MANUAL_EN	[12]	RW	* Transfer completed without ACK received (for manual mode only) * Note: After master-ID (HS mode), this bit should be asserted. 0: Disables 1: Enables	0x0000_0000
INT_TIMEOUT_AUTO_EN	[11]	RW	* Time out during auto mode transaction 0: Disables 1: Enables	0x0000_0000
INT_NO_DEV_AUTO_EN	[10]	RW	* No device responds the address ('Master does not select any device). (for auto mode only) 0: Disables 1: Enables	0x0000_0000
INT_NO_DEV_ACK_AUTO_EN	[9]	RW	* Device does not return ACK during master TX (for auto mode only) 0: Disables 1: Enables	0x0000_0000
INT_TRANS_ABORT_AUTO_EN	[8]	RW	* Lost arbitration during transaction (for auto mode only) 0: Disables 1: Enables	0x0000_0000
INT_TRANSFER_DONE_AUTO_EN	[7]	RW	* Command is successfully executed. This bit is automatically cleared by software read. (for auto mode only)	0x0000_0000

Name	Bit	Type	Description	Reset Value
			0: Disables 1: Enables	
INT_TRAILING_EN	[6]	RW	* Interrupt enable signal for trailing interrupt 0: Disables 1: Enables	0x0000_0000
INT_RX_OVERRUN_EN	[5]	RW	* Interrupt enable signal for RX overrun 0: Disables 1: Enables	0x0000_0000
INT_RX_UNDERRUN_EN	[4]	RW	* Interrupt enable signal for RX under run 0: Disables 1: Enables	0x0000_0000
INT_TX_OVERRUN_EN	[3]	RW	* Interrupt enable signal for TX overrun 0: Disables 1: Enables	0x0000_0000
RSVD0	[2]	RW	Reserved	0x0000_0000
INT_RX_ALMOSTFULL_EN	[1]	RW	* Interrupt enable signal for RX FIFO 0: Disables 1: Enables	0x0000_0000
INT_TX_ALMOSTEMPTY_EN	[0]	RW	* Interrupt enable signal for TX FIFO 0: Disables 1: Enables	0x0000_0000

4.2.9.2.1.5 INT_STAT

- Base Address: 0x4001_2000
- Address = Base Address + 0x0024, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
INT_SLAVE_ADDR_MATCH	[15]	RW	Write 1 to clear this bit. READ: (for slave mode only) I2C slave address is matched. 0: No interrupt occurred 1: Interrupt occurred	0x0000_0000
INT_LOSE_ARB_MANUAL	[14]	RW	Write 1 to clear this bit. READ: (for manual mode only) Lost arbitration during executing command 0: No interrupt occurred 1: Interrupt occurred	0x0000_0000
INT_TRANSFER_DONE_MANUAL	[13]	RW	Write 1 to clear this bit. READ: (for manual mode only)	0x0000_0000

Name	Bit	Type	Description	Reset Value
			One byte (data or address) is transmitted successfully, one byte data is received successfully or command (start or stop) is completed. 0: No interrupt occurred 1: Interrupt occurred * Note: In high-speed mode, completion of master-ID-transfer does not assert this bit.	
INT_TRANSFER_DONE_NOACK_MANUAL	[12]	RW	Write 1 to clear this bit. READ: (for manual mode only) Transfer completed without ACK received. 0: No interrupt occurred 1: Interrupt occurred * Note: After master-ID (HS mode), this bit must be asserted.	0x0000_0000
INT_TIMEOUT_AUTO	[11]	RW	Write 1 to clear this bit. READ: (for auto mode only) Time out during auto mode transaction. 0: No interrupt occurred 1: Interrupt occurred	0x0000_0000
INT_NO_DEV_AUTO	[10]	RW	Write 1 to clear this bit. READ: (for auto mode only) No device responds the address (Master does not select any device). 0: No interrupt occurred 1: Interrupt occurred	0x0000_0000
INT_NO_DEV_ACK_AUTO	[9]	RW	Write 1 to clear this bit. READ: (for auto mode only) Device does not return ACK during master TX. 0: No interrupt occurred 1: Interrupt occurred	0x0000_0000
INT_TRANS_ABORT_AUTO	[8]	RW	Write 1 to clear this bit. READ: (for auto mode only) Lost arbitration during transaction 0: No interrupt occurred 1: Interrupt occurred * Note: In high-speed mode, completion of master-ID-transfer does not assert this bit.	0x0000_0000
INT_TRANSFER_DONE_AUTO	[7]	RW	Write 1 to clear this bit. READ: (for auto mode only) Command is executed successfully. This bit is automatically cleared by software read. 0: No interrupt occurred 1: Interrupt occurred * Note: In high-speed mode, completion of master-ID-	0x0000_0000

Name	Bit	Type	Description	Reset Value
			transfer does not assert this bit.	
INT_TRAILING	[6]	RW	Write 1 to clear this bit. If HSI2C does not reach RX FIFO trigger level and does not receive data for TRAILING_CNT time, this interrupt is asserted, then the CPU must check the FIFO status and read out the rest. 0: No interrupt occurred 1: Interrupt occurred	0x0000_0000
INT_RX_OVERRUN	[5]	RW	Write 1 to clear this bit. READ: RX FIFO overrun error. 0: No error occurred 1: Overrun error occurred	0x0000_0000
INT_RX_UNDERRUN	[4]	RW	Write 1 to clear this bit. READ: RX FIFO underrun error 0: No error occurred 1: Underrun error occurred	0x0000_0000
INT_TX_OVERRUN	[3]	RW	Write 1 to clear this bit. READ: TX FIFO overrun error. 0: No error occurred 1: Overrun error occurred	0x0000_0000
RSVD0	[2]	RW	Reserved	0x0000_0000
INT_RXFIFO_ALMOST_FULL	[1]	RW	Write 1 to clear this bit. READ: 0: Data in RX FIFO is less than trigger level 1: Data in RX FIFO is more than trigger level	0x0000_0000
INT_TXFIFO_ALMOST_EMPTY	[0]	RW	Write 1 to clear this bit. READ: 0: Data in TX FIFO is more than trigger level 1: Data in TX FIFO is less than trigger level	0x0000_0000

NOTE:

1. I2C interrupt occurs when:

   Slave mode:

   The received slave address is matched with setting slave address in SFR I2C_ADDR.
   (HSI2C is selected by external I2C master)

   Master mode:

   Manual mode:

   Master lost arbitration

   Master completes one byte (either address or data) transfer but receives Not ACK (ACK bit is high)

   Master successfully accomplishes one byte transfer (ACK bit is low)

   Auto mode:

   No device acknowledges to the address

   Master receives Not ACK during transaction (this is master TX mode, slave device does not acknowledge current byte transfer).

   Transaction abort.

Transaction successfully completed.
Transaction timeout.

4.2.9.2.1.6 FIFO_STAT

- Base Address: 0x4001_2000
- Address = Base Address + 0x0030, Reset Value = 0x0100_0100

Name	Bit	Type	Description	Reset Value
RX_FIFO_EMPTY	[24]	R	* RX FIFO empty signal 0: Non-empty 1: Empty	0x0000_0001
RX_FIFO_FULL	[23]	R	* RX FIFO full signal 0: Non-full 1: Full	0x0000_0000
RX_FIFO_LEVEL	[22:16]	R	Data level in RX FIFO.	0x0000_0000
RSVD0	[15:9]	R	Reserved	0x0000_0000
TX_FIFO_EMPTY	[8]	R	* TX FIFO empty signal 0: Non-empty 1: Empty	0x0000_0001
TX_FIFO_FULL	[7]	R	* TX FIFO full signal 0: Non-full 1: Full	0x0000_0000
TX_FIFO_LEVEL	[6:0]	R	Data level in TX FIFO.	0x0000_0000

4.2.9.2.1.7 TXDATA

- Base Address: 0x4001_2000
- Address = Base Address + 0x0034, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
TXDATA	[31:0]	W	Transmit data buffer for HSI2C	0xDEAD_BEAF

4.2.9.2.1.8 RXDATA

- Base Address: 0x4001_2000
- Address = Base Address + 0x0038, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RXDATA	[31:0]	R	Received data buffer for HSI2C	0x0000_0000

4.2.9.2.1.9 I2C_CONF

- Base Address: 0x4001_2000
- Address = Base Address + 0x0040, Reset Value = 0x9803_C1FF

Name	Bit	Type	Description	Reset Value
AUTO_MODE	[31]	RW	* Auto flow control for I2C master 1: Auto control. I2C master automatically controls the whole transaction. 0: Manual control. Software manually controls transaction.	0x0000_0001
ADDRMODE	[30]	RW	1: 10-bit-address mode 0: 7-bit-address mode	0x0000_0000
HS_MODE	[29]	RW	* High-Speed Mode 0: Fast-mode 1: High-speed mode	0x0000_0000
FILTER_EN_SCL	[28]	RW	Enables SCL filter.	0x0000_0001
FILTER_EN_SDA	[27]	RW	Enables SDA filter.	0x0000_0001
RSVD0	[26:19]	RW	Reserved	0x0000_0000
FLT_CYCLE_SCL	[18:16]	RW	Glitch width to be removed for SCL.(number of clock cycles) If this field is 0, it works as if FILTER_EN_SCL were 0 (disabled).	0x0000_0003
FLT_CYCLE_SDA	[15:13]	RW	Glitch width to be removed for SDA.(number of clock cycles) If this field is 0, it works as if FILTER_EN_SDA were 0 (disabled).	0x0000_0006
RSVD1	[12:10]	RW	Reserved	0x0000_0000
STRCH_MANUAL	[9]	RW	Manually SCL stretch for slave. STRCH_EN should be 1 to make this bit effective.	0x0000_0000
STRCH_EN	[8]	RW	Enables slave SCL stretch	0x0000_0001
T_STOPTOIDLE	[7:0]	RW	STOP to IDLE state interval for I2C master	0x0000_00FF

4.2.9.2.1.10 I2C_AUTO_CONF

- Base Address: 0x4001_2000
- Address = Base Address + 0x0044, Reset Value = 0x0003_00FF

Name	Bit	Type	Description	Reset Value
MASTER_RUN	[31]	W	To start data transfer under I2C master mode, write 1 to this bit.	0x0000_0000
RSVD0	[30:18]	RW	Reserved	0x0000_0000
STOP_AFTER_TRANS	[17]	RW	For auto mode only. If this bit is set, i2c master asserts STOP condition after entire transaction is complete, either successful or failure.	0x0000_0001

Name	Bit	Type	Description	Reset Value
READ_WRTIE	[16]	RW	* Type of transaction (For auto mode only). 1: Read (RX) 0: Write (TX)	0x0000_0001
TRANS_LEN	[15:0]	RW	Length of Transaction. (Number of Bytes to RX or TX).	0x0000_00FF

4.2.9.2.1.11 I2C_TIMEOUT

- Base Address: 0x4001_2000
- Address = Base Address + 0x0048, Reset Value = 0x8000_00FF

Name	Bit	Type	Description	Reset Value
TIMEOUT_EN	[31]	RW	Enables timeout	0x0000_0001
RSVD0	[30:16]	RW	Reserved	0x0000_0000
TOUT_COUNT	[15:0]	RW	Timeout for master RX/TX	0x0000_00FF

4.2.9.2.1.12 I2C_MANUAL_CMD

- Base Address: 0x4001_2000
- Address = Base Address + 0x004C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
TX_DATA	[31:24]	RW	Specifies the data to be transmitted	0x0000_0000
RX_DATA	[23:16]	R	Specifies the received data	0x0000_0000
RX_ACK	[5]	RW	This is the Acknowledgement for master-RX. After software asserts READ_DATA, I2C master receives one byte from external i2c and sends one bit acknowledgement to external I2c.	0x0000_0000
READ_DATA	[4]	W	If you write 1 to this bit, it forces I2C master to receive one byte data. The data is then available in RX_DATA.	0x0000_0000
SEND_DATA	[3]	W	If you write 1 to this bit, it forces I2C master to send one byte data. The data should be pre-written in TX_DATA.	0x0000_0000
SEND_STOP	[2]	W	If you write 1 to this bit, it forces I2C master to send STOP condition.	0x0000_0000
SEND_RESTART	[1]	W	If you write 1 to this bit, it forces I2C master to send RE-START condition.	0x0000_0000
SEND_START	[0]	W	If you write 1 to this bit, it forces I2C master to send START condition.	0x0000_0000

NOTE: This Register is only valid in manual mode (AUTO_MODE is 0).

4.2.9.2.1.13 I2C_TRANS_STATUS

- Base Address: 0x4001_2000
- Address = Base Address + 0x0050, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
SLAVE_RW	[19]	R	* Current slave operation mode 1: TX mode 0: RX mode	0x0000_0000
STOP_COND	[18]	R	* Indicates stop condition on bus 1: Stop condition on bus 0: No stop condition on bus	0x0000_0000
MASTER_BUSY	[17]	R	* Indicates whether the data is transferring or not in master mode 1: The data is transferring 0: The data is not transferring	0x0000_0000
SLAVE_BUSY	[16]	R	* Indicates the data is transferring or not in slave mode 1: The data is transferring 0: The data is not transferring	0x0000_0000
SLAVE_SCL_STRETCH	[15]	R	* Indicates SCL is stretching or not in slave mode 1: SCL is stretching 0: SCL is not stretching	0x0000_0000
RSVD0	[14:0]	R	Reserved	0x0000_0000

NOTE:

1. MASTER BUSY: I2C master is busy executing transaction (for auto mode) or command (for manual mode). 'In auto mode, MASTER BUSY is high until all I2c transactions are completed. In manual mode, MASTER BUSY is High until the current command is completed.
2. SLAVE BUSY: High when I2C slave is receiving Address or when data is transferring.

4.2.9.2.1.14 I2C_TIMING_HS1

- Base Address: 0x4001_2000
- Address = Base Address + 0x0054, Reset Value = 0x0F0F_0F00

Name	Bit	Type	Description	Reset Value
TSTART_SU_HS	[31:24]	RW	Start condition setup timing. (Start condition after SCL rising-edge)	0x0000_000F
TSTART_HD_HS	[23:16]	RW	Start condition hold timing. (Start condition leads to SCL falling-edge)	0x0000_000F
TSTOP_SU_HS	[15:8]	RW	STOP condition setup timing. (STOP condition after SCL rising-edge)	0x0000_000F
TSDA_SU_HS	[7:0]	RW	SDA trigger timing (output setup timing) • If this field is lesser than or equal to (TSCL_L_HS/2) or greater than TSCL_L_HS, it has no effects and default	0x0000_0000

Name	Bit	Type	Description	Reset Value
			trigger timing is used. Effective range is determined using the following equation; (TSCL_L_HS/2) < TSDA_SU_HS <= TSCL_L_HS • To enhance setup timing in maximum frequency operation of high-speed mode, it is recommended to use closer value or same value as TSCL_L_HS (maximum effective value). • If the FLT_CYCLE_SCL is a higher value, it covers almost of half period of SCL low interval. And, by default, SDA triggering (changing) time is the half of TSCL_L_HS(FS). Without this bit field, SDA trigger time is NOT changeable, so that SDA is always triggered near SCL rising edge instead of the center of SCL low interval. TSDA_SU_HS can move SDA trigger time faster to the center of SCL low interval.	

4.2.9.2.1.15 I2C_TIMING_HS2

- Base Address: 0x4001_2000
- Address = Base Address + 0x0058, Reset Value = 0x0F0F_FFFF

Name	Bit	Type	Description	Reset Value
TDATA_SU_HS	[31:24]	RW	Data setup timing	0x0000_000F
RSVD0	[23:16]	RW	Reserved	0x0000_000F
TSCL_L_HS	[15:8]	RW	SCL low period	0x0000_00FF
TSCL_H_HS	[7:0]	RW	SCL high period	0x0000_00FF

4.2.9.2.1.16 I2C_TIMING_HS3

- Base Address: 0x4001_2000
- Address = Base Address + 0x005C, Reset Value = 0x00FF_00FF

Name	Bit	Type	Description	Reset Value
CLK_DIV	[23:16]	RW	The PCLK divider factor when working in HS-mode.	0x0000_00FF
RSVD0	[15:8]	RW	Reserved	0x0000_0000
TSR_RELEASE	[7:0]	RW	RE-START condition	0x0000_00FF

4.2.9.2.1.17 I2C_TIMING_FS1

- Base Address: 0x4001_2000
- Address = Base Address + 0x0060, Reset Value = 0x0F0F_0F00

Name	Bit	Type	Description	Reset Value
TSTART_SU_FS	[31:24]	RW	Start Condition setup timing.	0x0000_000F

Name	Bit	Type	Description	Reset Value
			(Start condition after SCL rising-edge)	
TSTART_HD_FS	[23:16]	RW	Start Condition Hold timing. (Start condition leads to SCL falling-edge)	0x0000_000F
TSTOP_SU_FS	[15:8]	RW	STOP condition setup timing. (STOP condition after SCL rising-edge)	0x0000_000F
TSDA_SU_FS	[7:0]	RW	SDA trigger timing (output setup timing) - If this field is lesser than or equal to (TSCL_L_FS/2) or greater than TSCL_L_FS, it has no effects and default trigger timing is used. Effective range is determined using the following equation; (TSCL_L_FS/2) <= TSDA_SU_FS <= TSCL_L_FS - It is recommended to use the reset value because it is not critical in fast-speed mode.	0x0000_0000

4.2.9.2.1.18 I2C_TIMING_FS2

- Base Address: 0x4001_2000
- Address = Base Address + 0x0064, Reset Value = 0x0F0F_FFFF

Name	Bit	Type	Description	Reset Value
TDATA_SU_FS	[31:24]	RW	Data setup timing	0x0000_000F
RSVD0	[23:16]	RW	Reserved	0x0000_000F
TSCL_L_FS	[15:8]	RW	SCL low period	0x0000_00FF
TSCL_H_FS	[7:0]	RW	SCL high period	0x0000_00FF

4.2.9.2.1.19 I2C_TIMING_FS3

- Base Address: 0x4001_2000
- Address = Base Address + 0x0068, Reset Value = 0x00FF_00FF

Name	Bit	Type	Description	Reset Value
CLK_DIV	[23:16]	RW	The PCLK divider factor when working in fast mode for I2C communications.	0x0000_00FF
RSVD0	[15:8]	RW	Reserved	0x0000_0000
TSR_RELEASE	[7:0]	RW	RE-START condition	0x0000_00FF

4.2.9.2.1.20 I2C_TIMING_SLA

- Base Address: 0x4001_2000
- Address = Base Address + 0x006C, Reset Value = 0x0000_00FF

Name	Bit	Type	Description	Reset Value
I2C_TIMING_SLA	[15:0]	RW	Data hold timing for I2C slave. (data transition after SCL falling-edge) (For both auto and manual modes)	0x0000_00FF

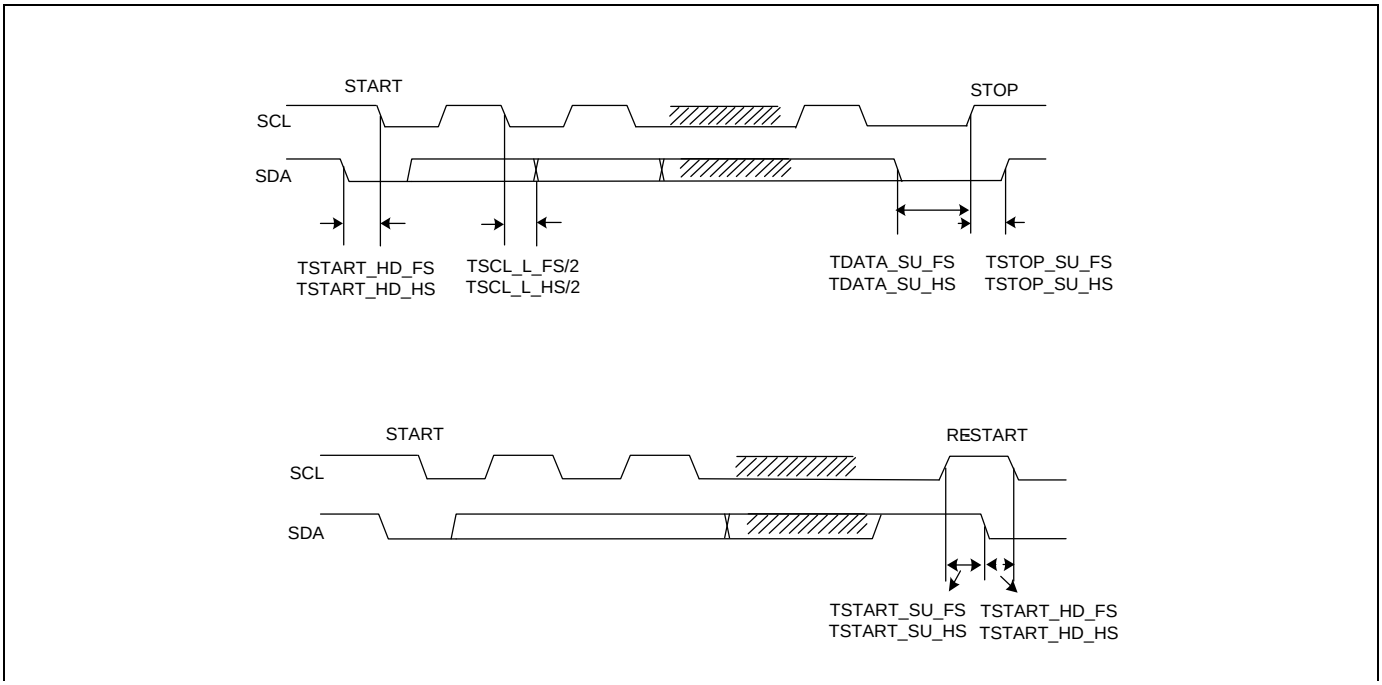
NOTE: The value of TDATA_HD should be less than the value of SCL_period/(2 × PCLK_period).

4.2.9.2.1.21 I2C_ADDR

- Base Address: 0x4001_2000
- Address = Base Address + 0x0070, Reset Value = 0xFF0F_FFFF

Name	Bit	Type	Description	Reset Value
MASTERID	[31:24]	RW	Master ID for I2C master. (For AUTO mode and HS mode).	0x0000_00FF
RSVD0	[23:20]	RW	Reserved	0x0000_0000
SLAVE_ADDR_MAS	[19:10]	RW	Slave address bit [9:0] for I2C master (for AUTO mode only).	0x0000_03FF
SLAVE_ADDR_SLA	[9:0]	RW	Slave address bit [9:0] for I2C slave.	0x0000_03FF

Figure 4-30 and *Figure 4-31* illustrate the relationship of timing parameters.



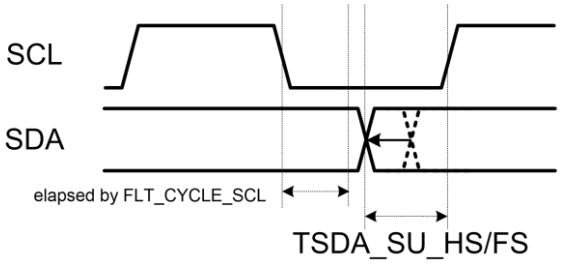


Figure 4-30 I2C Master Timing Diagram

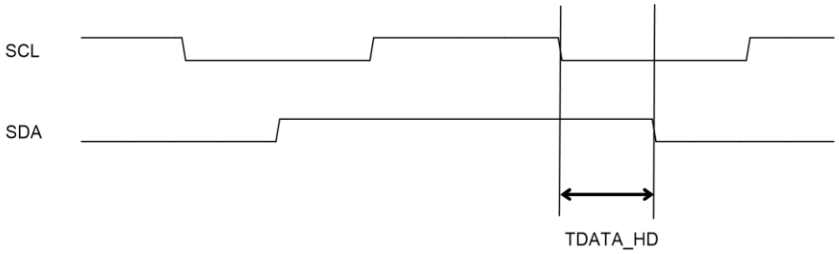


Figure 4-31 I2C Slave Timing Diagram

4.2.10 Serial Peripheral Interface

Serial Peripheral Interface (SPI) is the ARM PrimeCell PL022 Synchronous Serial Port (SSP). It enables synchronous serial communications with peripheral devices that have either a Motorola SPI compatible interface, Texas Instruments Synchronous Serial interface, or National Semiconductor Microwire interface. SPI can behave as a master or a slave interface and can perform parallel-to-serial conversion on data written to an internal 16-bit wide and 8-deep transmit FIFO. It also performs serial-to-parallel conversion on the serial input data and buffers it in a receive FIFO which is 16-bit wide and 8-deep. SPI asserts interrupts to request transmit and receive buffers service to indicate an overrun or receive timeout condition in the receive FIFO. A block diagram of the SPI is illustrated in *Figure 4-32*. The APB interface generates decoded write signals for registers in the device. The Register block contains the registers in the SSP. The control information written into the SSPCR0 and the SSPCPSR registers is synchronized to the SSPCLK clock domain through synchronization control logic located in the Register block and in the Clock prescaler.

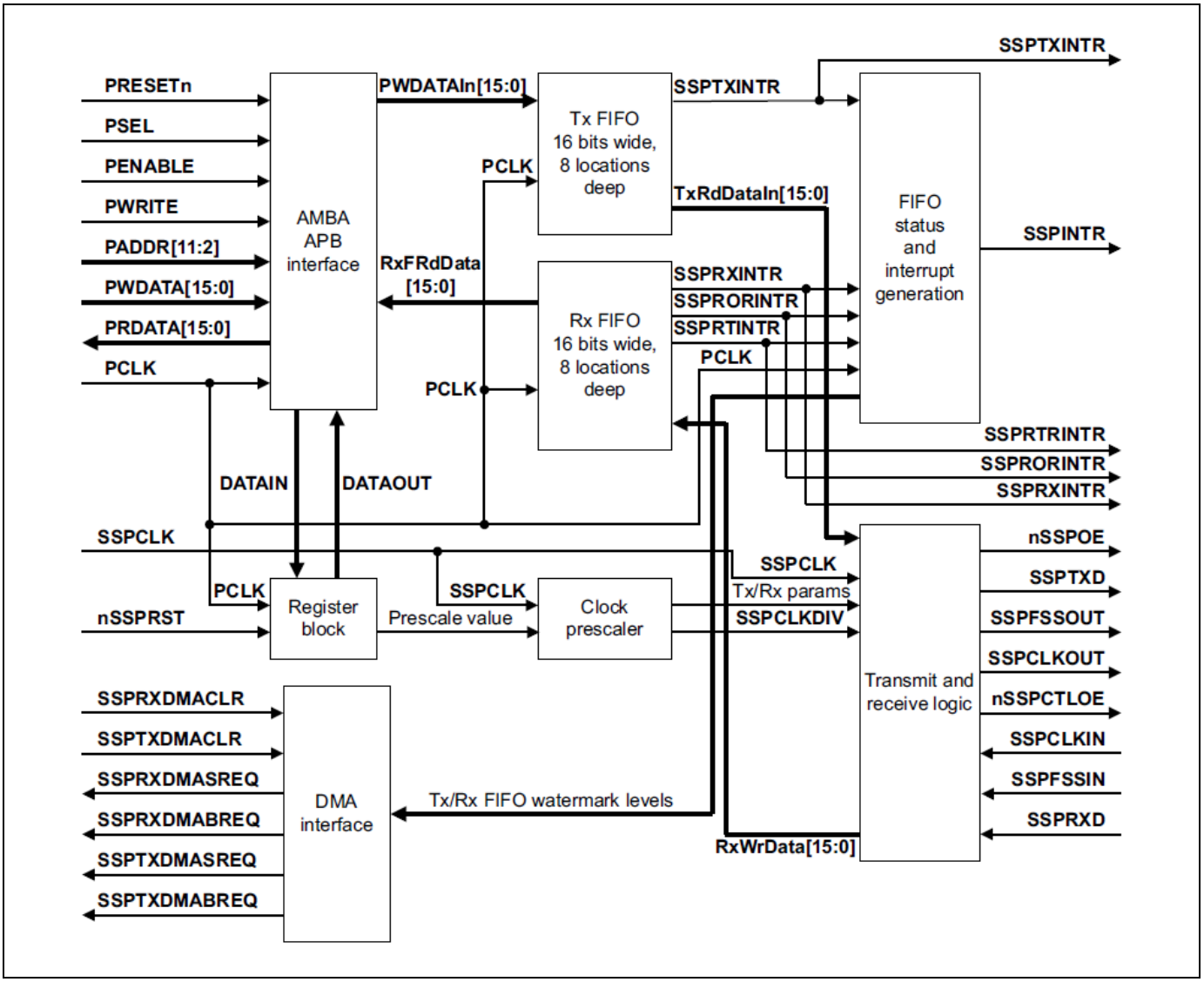


Figure 4-32 Block Diagram of SPI

When the MS bit in the SSPCR1 register is cleared, the SSP behaves as a master. When the bit is set, the SSP behaves as a slave. In the Slave mode, the SSP acts as a receive-only slave when the SOD bit in the SSPCR1 register is set. When cleared, it can also transmit. In the master mode, SSPCLK is first divided by the programmed pre-scale value and then by the SCR value to generate the SSPCLKOUT signal. In the slave mode, the slave interface uses the SSPFSSIN and SSPCLKIN signals from the external master. The transmitter, in accordance with the transmission parameters programmed into the control registers, converts data written in to the Transmit FIFO into a serial bit stream on the SSPTXD output line. The receiver performs serial-to-parallel conversion on data received on the SSPRXD line. Received data is buffered in the 16-bit wide 8-deep receive FIFO. The Transmit FIFO and the Receive FIFO are 16-bits wide and 8-deep. They generate the service requests, SSPTXINTR and SSPRXINTR. The Receive FIFO also generates the Receive Overrun Interrupt signal, SSPRORINTR and the Receive Timeout Interrupt signal, SSPRTINTR. The interrupt generation block uses the SSPTXINTR, SSPRXINTR, SSPRORINTR, and SSPRTINTR signals to generate the combined interrupt, SSPINTR.

4.2.10.1 Functional Description of SPI

This section describes the following topics.

- Interface reset
- Configuring the SSP
- Enable PrimeCell SSP operation
- Clock ratios
- Programming the SSPCR0 control register
- Programming the SSPCR1 control register
- Frame format
- Texas Instruments synchronous serial frame format
- Motorola SPI frame format
- Motorola SPI Format with SPO=0, SPH=0
- Motorola SPI Format with SPO=0, SPH=1
- Motorola SPI Format with SPO=1, SPH=0
- Motorola SPI Format with SPO=1, SPH=1
- National Semiconductor Microwire frame format
- Examples of master and slave configurations
- PrimeCell DMA interface

4.2.10.1.1 Interface Reset

The PrimeCell SSP is reset by the global reset signal, PRESETn, and a block-specific reset signal, nSSPRST. An external reset controller must use PRESETn to assert nSSPRST asynchronously and negate it synchronously to SSPCLK. PRESETn must be asserted LOW for a period long enough to reset the slowest block in the on-chip system, and then taken HIGH again. The PrimeCell SSP requires PRESETn to be asserted LOW for at least one period of PCLK.

4.2.10.1.2 Configuring the SSP

Following reset, the PrimeCell SSP logic is disabled and must be configured when in this state. It is necessary to program control registers SSPCR0 and SSPCR1 to configure the peripheral as a master or slave operating under one of the following protocols:

- Motorola SPI
- Texas Instruments SSI
- National Semiconductor.

The bit rate, derived from the external SSPCLK, requires the programming of the clock prescale register SPCPSR. See Clock prescale register, SSPCPSR.

4.2.10.1.3 Enable PrimeCell SSP Operation

You can either prime the transmit FIFO, by writing up to eight 16-bit values when the PrimeCell SSP is disabled, or permit the transmit FIFO service request to interrupt the CPU. Once enabled, transmission or reception of data begins on the transmit, SSPTXD, and receive, SSPRXD, pins.

4.2.10.1.4 Clock Ratios

There is a constraint on the ratio of the frequencies of PCLK to SSPCLK. The frequency of SSPCLK must be less than or equal to that of PCLK. This ensures that control signals from the SSPCLK domain to the PCLK domain are guaranteed to get synchronized before one frame duration:

$$F_{SSPCLK} <= F_{PCLK}$$

In the slave mode of operation, the SSPCLKIN signal from the external master is double-synchronized and then delayed to detect an edge. It takes three SSPCLKs to detect an edge on SSPCLKIN. SSPTXD has less setup time to the falling edge of SSPCLKIN on which the master is sampling the line.

The setup and hold times on SSPRXD, with reference to SSPCLKIN, must be more conservative to ensure that it is at the right value when the actual sampling occurs within the SSPMS. To ensure correct device operation, SSPCLK must be at least 16 times faster than the maximum expected frequency of SSPCLKIN.

The frequency selected for SSPCLK must accommodate the desired range of bit clock rates. The ratio of minimum SSPCLK frequency to SSPCLKOUT maximum frequency in the case of the slave mode is 16, and for the master mode, it is two.

To generate a maximum bit rate of 51.2Mbps in the master mode, the frequency of SSPCLK must be at least 102.4 MHz. With an SSPCLK frequency of 102.4MHz, the SSPCPSR register must be programmed with a value of 2, and the SCR[7:0] field in the SSPCR0 register must be programmed with a value of 0.

To work with a maximum bit rate of 6.4Mbps in the slave mode, the frequency of SSPCLK must be at least 102.4MHz. With an SSPCLK frequency of 102.4MHz, the SSPCPSR register can be programmed with a value of 16, and the SCR[7:0] field in the SSPCR0 register can be programmed with a value of 0. Similarly, the ratio of SSPCLK maximum frequency to SSPCLKOUT minimum frequency is 254 x 256. See Control register 0, SSPCR0 and Clock prescale register, SSPCPSR

The minimum frequency of SSPCLK is governed by the following equations, both of which must be satisfied:

$$F_{SSPCLK}(min) => 2 \times F_{SSPCLKOUT}(max), \text{ for master mode}$$
$$F_{SSPCLK}(min) => 16 \times F_{SSPCLKIN}(max), \text{ for slave mode.}$$

The maximum frequency of SSPCLK is governed by the following equations, both of which must be satisfied:

$$F_{SSPCLK}(max) <= 254 \times 256 \times F_{SSPCLKOUT}(min), \text{ for master mode}$$
$$F_{SSPCLK}(max) <= 254 \times 256 \times F_{SSPCLKIN}(min), \text{ for slave mode.}$$

4.2.10.1.5 Programming the SSPCR0 Control Register

See Control register 0, SSPCR0 for more information on the bit assignment of this register.

The SSPCR0 register is used to:

- program the serial clock rate
- select one of the three protocols
- select the data word size, where applicable.

The Serial Clock Rate (SCR) value, in conjunction with the SSPCPSR clock prescale divisor value, CPSDVSR, is used to derive the PrimeCell SSP transmit and receive bit rate from the external SSPCLK.

The frame format is programmed through the FRF bits, and the data word size through the DSS bits.

Bit phase and polarity, applicable to Motorola SPI format only, are programmed through the SPH and SPO bits.

4.2.10.1.6 Programming the SSPCR1 Control Register

See Control register 1, SSPCR1, for more information on the bit assignment of this register.

The SSPCR1 register is used to:

- select master or slave mode
- enable a loop back test feature
- enable the PrimeCell SSP peripheral

To configure the PrimeCell SSP as a master, clear the SSPCR1 register master or slave selection bit, MS, to 0. This is the default value on reset.

Setting the SSPCR1 register MS bit to 1 configures the PrimeCell SSP as a slave. When configured as a slave, enabling or disabling of the PrimeCell SSP SSPTXD signal is provided through the SSPCR1 slave mode SSPTXD output disable bit, SOD. You can use this in some multi-slave environments where masters might parallel broadcast.

To enable the operation of the PrimeCell SSP, set the Synchronous Serial Port Enable (SSE) bit to 1.

Bit Rate Generation

The serial bit rate is derived by dividing down the input clock, SSPCLK. The clock is first divided by an even prescale value CPSDVSR in the range 2-254, and is programmed in SSPCPSR. The clock is divided again by a value in the range 1-256, that is 1 + SCR, where SCR is the value programmed in SSPCR0.

The following equation defines the frequency of the output signal bit clock, SSPCLKOUT:

$$F_{SSPCLKOUT} = \frac{F_{SSPCLK}}{\mathbf{CPSDVR} \times (\mathbf{1} + \mathbf{SCR})}$$

For example, if SSPCLK is 102.4MHz, and CPSDVSR = 2, then SSPCLKOUT has a frequency range from 200kHz to 51.2MHz.

4.2.10.1.7 Frame Format

Each data frame is between 4-16 bits long, depending on the size of data programmed, and is transmitted starting with the MSB. You can select the following basic frame types:

- Texas Instruments synchronous serial
- Motorola SPI
- National Semiconductor Microwire

For all formats, the serial clock, SSPCLKOUT, is held inactive while the PrimeCell SSP is idle, and transitions at the programmed frequency only during active transmission or reception of data. The idle state of SSPCLKOUT is utilized to provide a receive timeout indication that occurs when the receive FIFO still contains data after a timeout period.

For Motorola SPI and National Semiconductor Microwire frame formats, the serial frame, SSPFSSOUT, pin is active-LOW, and is asserted, pulled-down, during the entire transmission of the frame.

For Texas Instruments synchronous serial frame format, the SSPFSSOUT pin is pulsed for one serial clock period, starting at its rising edge, prior to the transmission of each frame. For this frame format, both the PrimeCell SSP and the off-chip slave device drive their output data on the rising edge of SSPCLKOUT, and latch data from the other device on the falling edge.

Unlike the full-duplex transmission of the other two frame formats, the National Semiconductor Microwire format uses a special master-slave messaging technique that operates at half-duplex. In this mode, when a frame begins, an 8-bit control message is transmitted to the off-chip slave. During this transmission, the SSS receives no incoming data. After the message has been sent, the off-chip slave decodes it and, after waiting one serial clock after the last bit of the 8-bit control message has been sent, responds with the requested data. The returned data can be 4-16 bits in length, making the total frame length in the range 13-25 bits.

4.2.10.1.7.1 Texas Instruments Synchronous Serial Frame Format

Figure 4-33 illustrates the Texas Instruments synchronous serial frame format for a single transmitted frame.

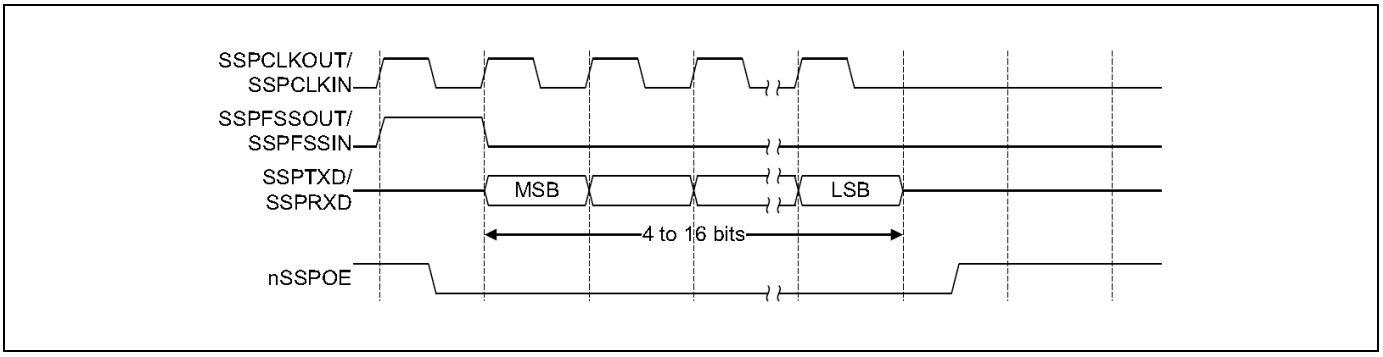


Figure 4-33 Texas Instruments Synchronous Serial Frame Format, Single Transfer

In this mode, SSPCLKOUT and SSPFSSOUT are forced LOW, and the transmit data line, SSPTXD is tristated whenever the PrimeCell SSP is idle. When the bottom entry of the transmit FIFO contains data, SSPFSSOUT is pulsed High for one SSPCLKOUT period. The value to be transmitted is also transferred from the transmit FIFO to the serial shift register of the transmit logic. On the next rising edge of SSPCLKOUT, the MSB of the 4-bit to 16-bit data frame is shifted out on the SSPTXD pin. In a similar way, the MSB of the received data is shifted onto the SSPRXD pin by the off-chip serial slave device.

Both PrimeCell SSP and off-chip slave device drive their output data on the rising edge of SSPCLKOUT, and latch data from the other device on the falling edge. The received data is transferred from the serial shifter to the receive FIFO on the first rising edge of PCLK after the LSB has been latched.

Figure 4-34 illustrates the Texas Instruments synchronous serial frame format when back-to-back frames are transmitted.

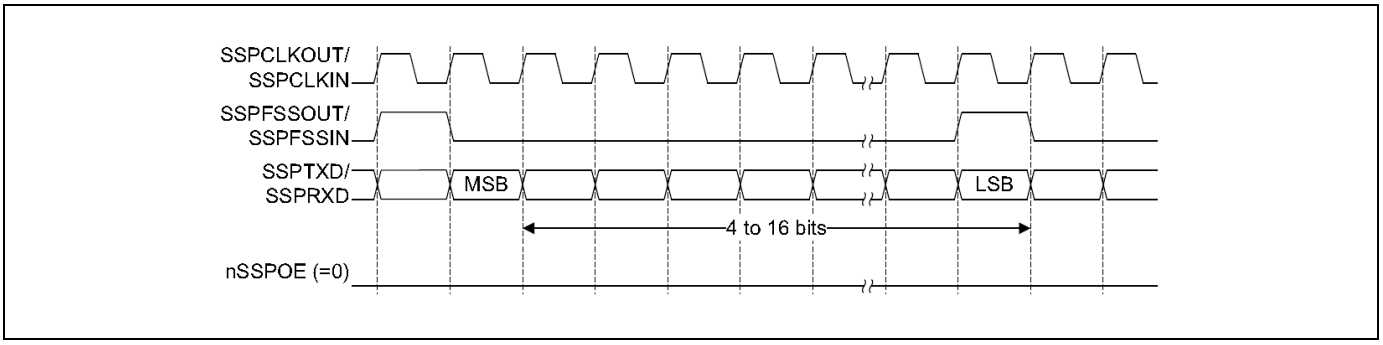


Figure 4-34 Texas Instruments Synchronous Serial Frame Format, Continuous Transfer

4.2.10.1.7.2 Motorola SPI Frame Format

The Motorola SPI interface is a four-wire interface where the SSPFSSOUT signal behaves as a slave select. The main feature of the Motorola SPI format is that you can program the inactive state and phase of the SSPCLKOUT signal using the SPO and SPH bits of the SSPSCR0 control register. For more information, refer Control register 0, SSPCR0.

SPO, Clock Polarity

When the SPO clock polarity control bit is Low, it produces a steady state Low value on the SSPCLKOUT pin. If the SPO clock polarity control bit is High, a steady state High value is placed on the SSPCLKOUT pin when data is not being transferred.

SPH, Clock Phase

The SPH control bit selects the clock edge that captures data and enables it to change state. It has the most impact on the first bit transmitted by either permitting or not permitting a clock transition before the first data capture edge.

When the SPH phase control bit is Low, data is captured on the first clock edge transition.

When the SPH clock phase control bit is High, data is captured on the second clock edge transition.

4.2.10.1.7.2.1 Motorola SPI Format with SPO=0, SPH=0

Figure 4-35 and *Figure 4-36* illustrate single and continuous transmission signal sequences for Motorola SPI format with SPO=0, SPH=0. *Figure 4-35* illustrates a single transmission signal sequence for Motorola SPI frame format with SPO=0, SPH=0.

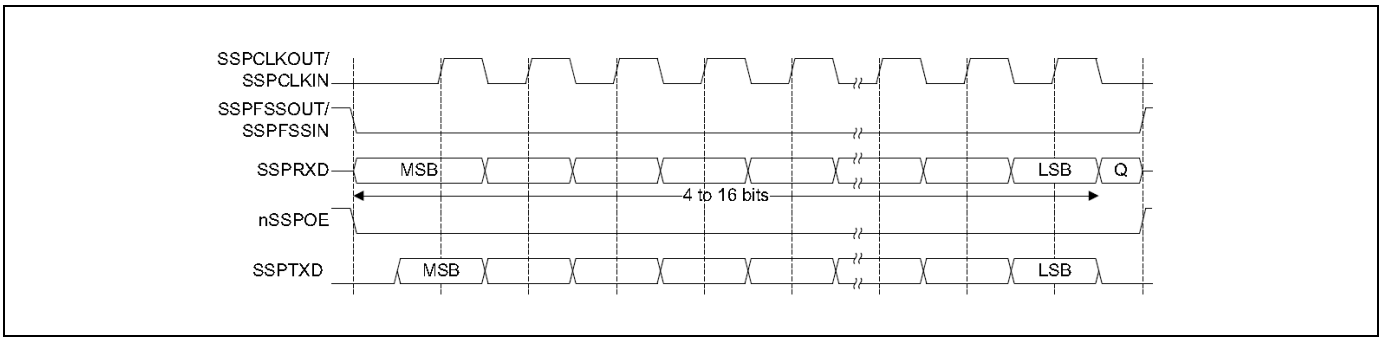


Figure 4-35 Motorola SPI Frame Format, Single Transfer, with SPO = 0 and SPH = 0

Figure 4-36 illustrates a continuous transmission signal sequence for Motorola SPI frame format with SPO=0, SPH=0

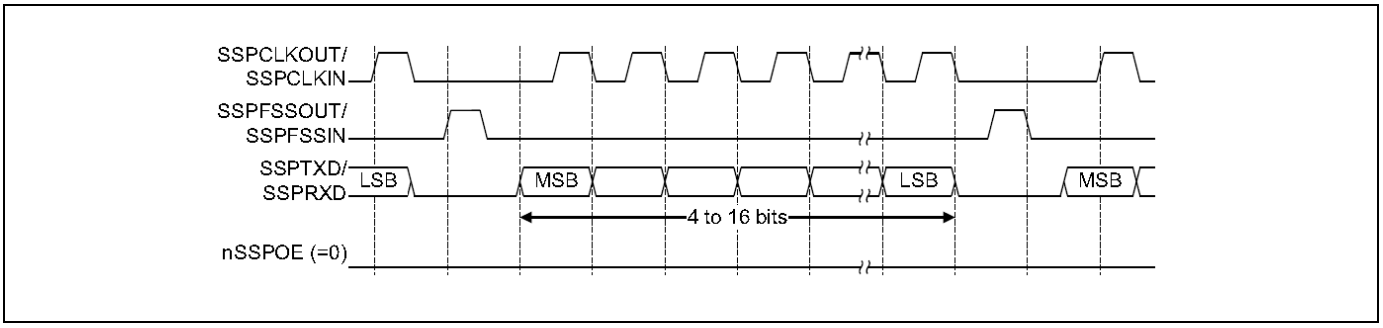


Figure 4-36 Motorola SPI Frame Format, Continuous Transfer, with SPO = 0 and SPH = 0

4.2.10.1.7.2.2 Motorola SPI Format with SPO=0, SPH=1

Figure 4-37 illustrates the transfer signal sequence for Motorola SPI format with SPO=0, SPH=1, and it covers both single and continuous transfers.

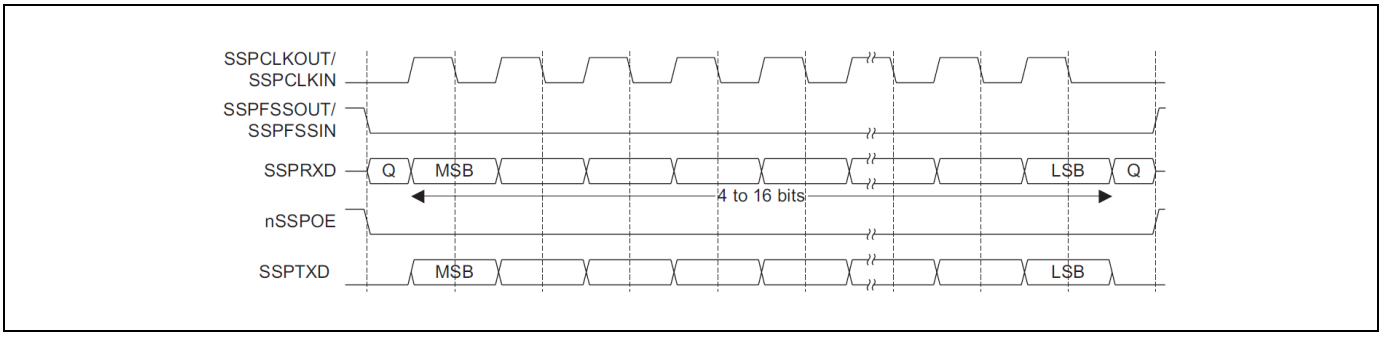


Figure 4-37 Motorola SPI Frame Format with SPO = 0 and SPH = 1, Single and Continuous Transfers

4.2.10.1.7.2.3 Motorola SPI Format with SPO=1, SPH=0

Figure 4-38 and *Figure 4-39* illustrate single and continuous transmission signal sequences for Motorola SPI format with SPO=1, SPH=0.

Figure 4-38 illustrates a single transmission signal sequence for Motorola SPI format with SPO=1, SPH=0.

In *Figure 4-38*, Q is an undefined signal.

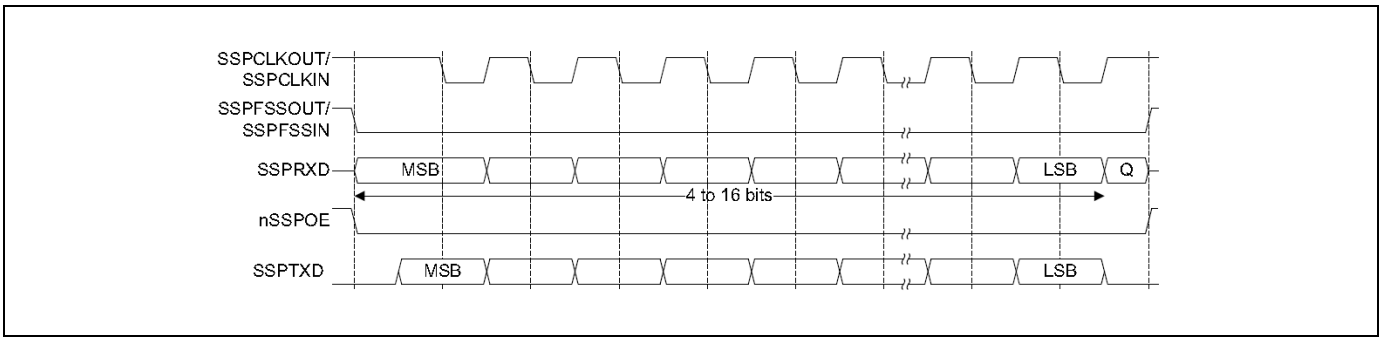


Figure 4-38 Motorola SPI Frame Format, Single Transfer, with SPO = 1 and SPH = 0

Figure 4-39 illustrates a continuous transmission signal sequence for Motorola SPI format with SPO=1, SPH=0

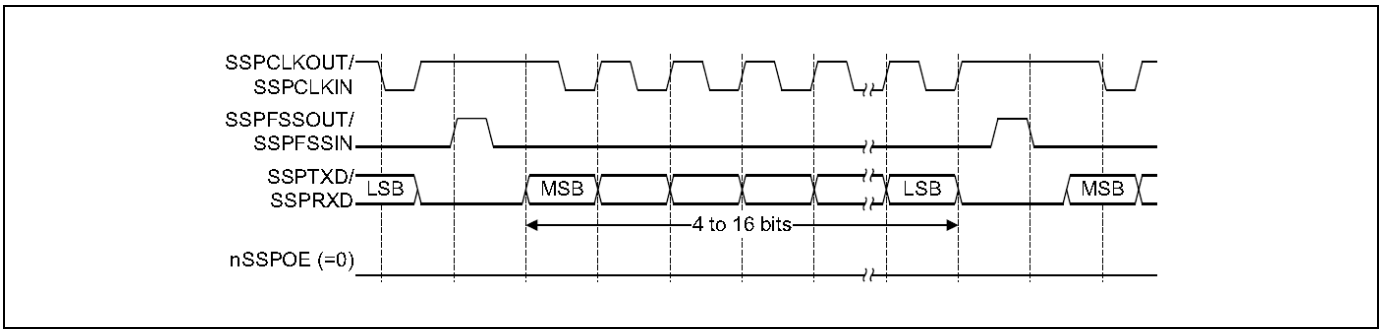


Figure 4-39 Motorola SPI Frame Format, Continuous Transfer, with SPO = 1 and SPH = 0

4.2.10.1.7.2.4 Motorola SPI Format with SPO=1, SPH=1

Figure 4-40 illustrates the transfer signal sequence for Motorola SPI format with SPO=1, SPH=1, and it covers both single and continuous transfers.

In *Figure 4-40*, Q is an undefined signal.

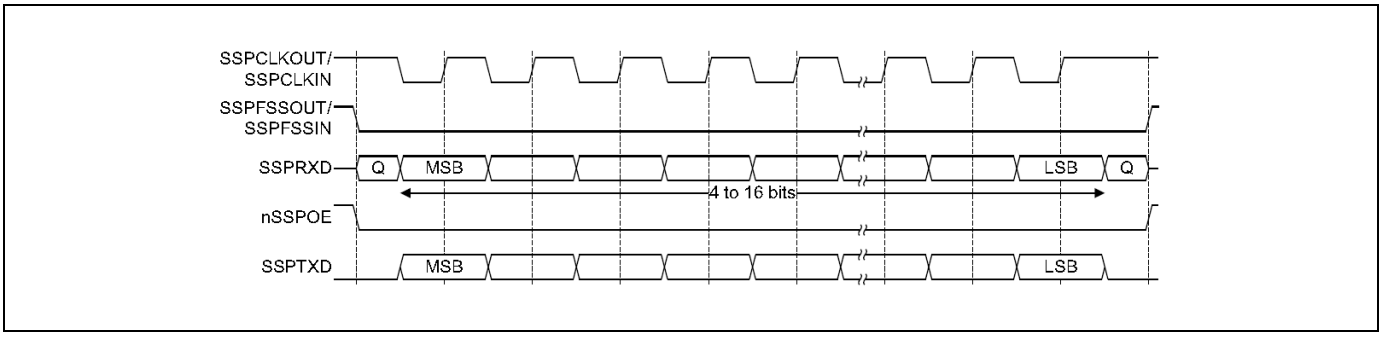


Figure 4-40 Motorola SPI Frame Format with SPO = 1 and SPH = 1, Single and Continuous Transfers

4.2.10.1.7.3 National Semiconductor Microwire Frame Format

Figure 4-41 illustrates the National Semiconductor Microwire frame format for a single frame.

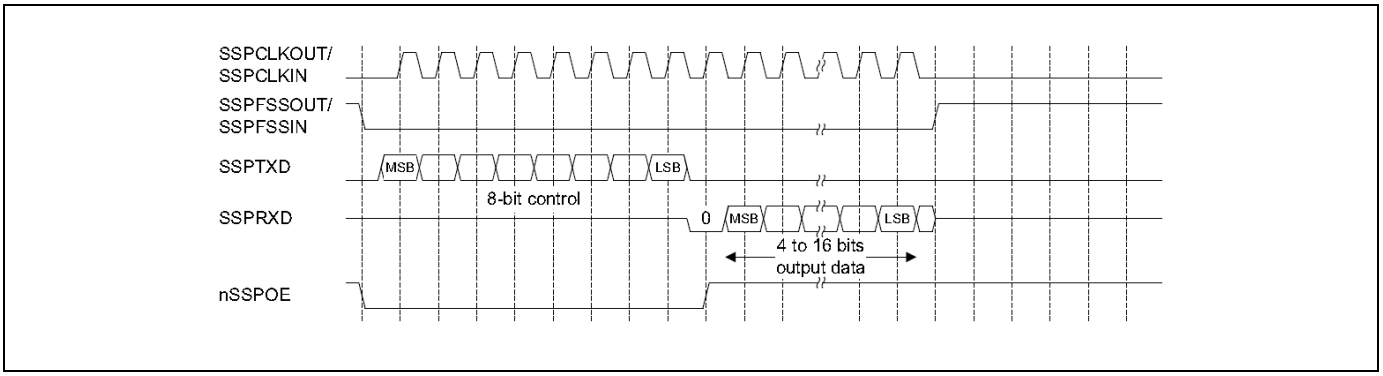


Figure 4-41 Microwire Frame Format, Single Transfer

Microwire format is very similar to SPI format, except that transmission is half-duplex instead of full-duplex, using a master-slave message passing technique. Each serial transmission begins with an 8-bit control word that is transmitted from the PrimeCell SSP to the off-chip slave device. During this transmission, the PrimeCell SSP receives no incoming data. After the message has been sent, the off-chip slave decodes it and, after waiting one serial clock after the last bit of the 8-bit control message has been sent, responds with the required data. The returned data is 4 to 16 bits in length, making the total frame length in the range 13-25 bits.

NOTE: The off-chip slave device can tristate the receive line either on the falling edge of SSPCLKOUT after the LSB has been latched by the receive shifter or when the SSPFSSOUT pin goes High.

For continuous transfers, data transmission begins and ends in the same manner as a single transfer. However, the SSPFSSOUT line is continuously asserted, held Low, and transmission of data occurs back-to-back. The control byte of the next frame directly follows after the LSB of the received data from the current frame. Each of the received values is transferred from the receive shifter on the falling edge SSPCLKOUT, after the LSB of the frame has been

latched into the PrimeCell SSP.

Figure 4-42 illustrates the National Semiconductor Microwire frame format when back-to-back frames are transmitted.

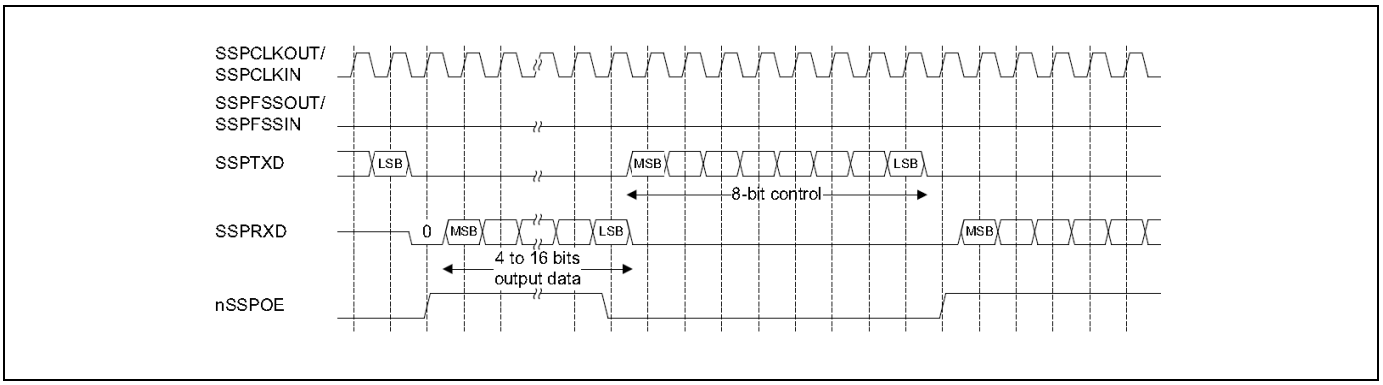


Figure 4-42 Microwire Frame Format, Continuous Transfers

In Microwire mode, the PrimeCell SSP slave samples the first bit of receive data on the rising edge of SSPCLKIN after SSPFSSIN has gone LOW. Masters that drive a free-running SSPCKLIN must ensure that the SSPFSSIN signal has sufficient setup and hold margins with respect to the rising edge of SSPCLKIN.

Figure 4-43 illustrates setup and hold time requirements.

For the SSPCLKIN rising edge on which the PrimeCell SSP slave samples the first bit of receive data, SSPFSSIN must have a setup of at least two times the period of SSPCLK on which the PrimeCell SSP operates.

For the SSPCLKIN rising edge prior to this edge, SSPFSSIN must have a hold of at least one SSPCLK period.

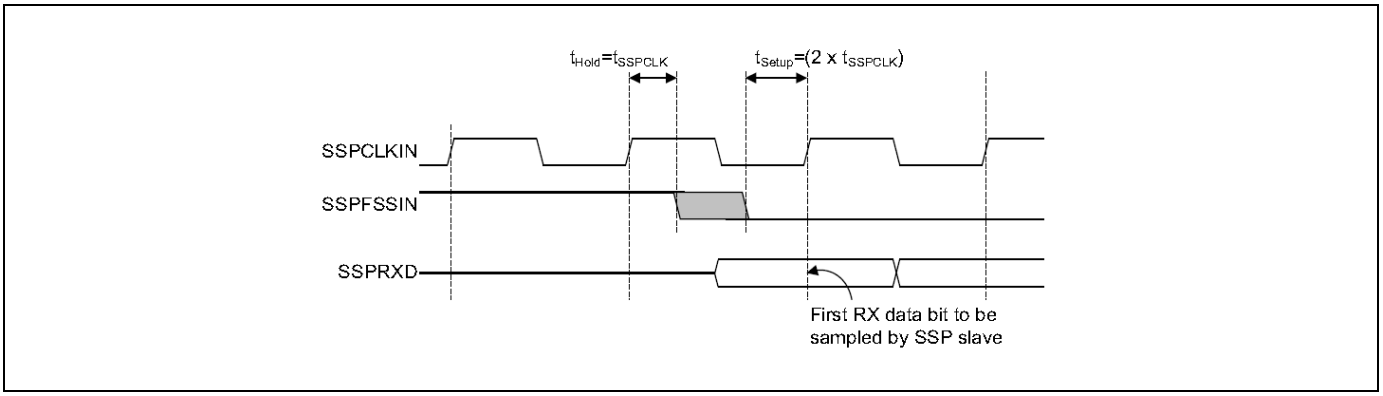


Figure 4-43 Microwire Frame Format, SSPFSSIN Input Setup and Hold Requirements

4.2.10.1.8 PrimeCell DMA Interface

The PrimeCell SSP provides an interface to connect to the DMA controller. The PrimeCell SSP DMA control register, SSPDMACR controls the DMA operation of the PrimeCell SSP. For more information, refer Chapter *4.2.10.2.1.10 SSPDMACLR*.

Receive

The DMA interface includes the following signals, for receive:

SSPRXDMASREQ:

Single-character DMA transfer request that is asserted by the SSP. This signal is asserted when the receive FIFO contains at least one character.

SSPRXDMABREQ:

Burst DMA transfer request that is asserted by the SSP. This signal is asserted when the receive FIFO contains RXIFLSEL or more characters.

SSPRXDMACR:

DMA request clear that is asserted by the DMA controller to clear the receive request signals. If DMA burst transfer is requested, the clear signal is asserted during the transfer of the last data in the burst.

Transmit

The DMA interface includes the following signals, for transmit:

SSPTXDMASREQ:

Single-character DMA transfer request that is asserted by the SSP. This signal is asserted when there is at least one empty location in the transmit FIFO.

SSPTXDMABREQ

Burst DMA transfer request that is asserted by the SSP. This signal is asserted when the transmit FIFO contains TXIFLSEL or fewer.

SSPTXDMACR:

DMA request clear that is asserted by the DMA controller to clear the transmit request signals. If a DMA burst transfer is requested, the clear signal is asserted during the transfer of the last data in the burst.

The burst transfer and single transfer request signals are not mutually exclusive. They can both be asserted at the same time. For example, when there is less data than the trigger level in the transmit FIFO, the burst transfer request and single transfer request are asserted. When the amount of data left in the transmit FIFO is more than trigger level but not full, only the single request is asserted.

Each request signal remains asserted until the relevant DMA clear signal is asserted. After the request clear signal is deasserted, a request signal can become active again, depending on the conditions described above. All request signals are deasserted if the PrimeCell SSP is disabled or the DMA enable signal is cleared. *Table 4-6* describes DMA/INT trigger point for the transmit and receive FIFOs

Table 4-6 DMA/INT Trigger Point for the Transmit and Receive FIFOs

Trigger Point	
Transmit, Number of empty locations	Receive, Number of Filled Locations
4, 6, 7	1, 2, 4

Figure 4-44 illustrates the timing diagram for both a single transfer request and a burst transfer request, with the appropriate DMA clear signal. The signals are all synchronous to PCLK.

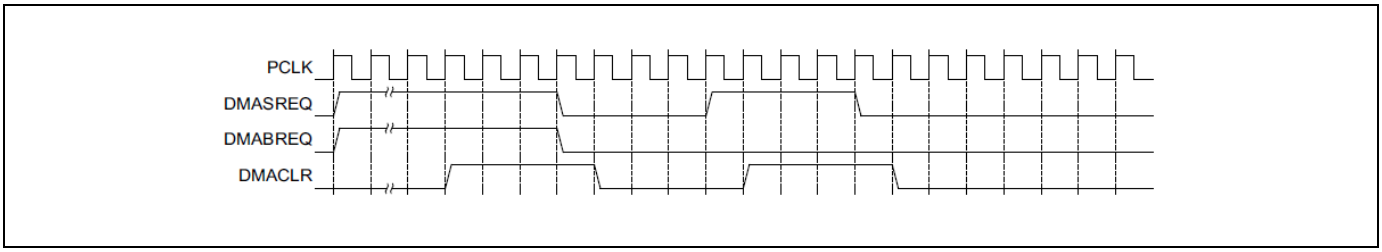


Figure 4-44 DMA Transfer Waveforms

4.2.10.2 Register Description

4.2.10.2.1 Register Map Summary

- Base Address: 0x4000_D000

Register	Offset	Description	Reset Value
SSPCR0	0x0000	Control Register 0	0x0000_0000
SSPCR1	0x0004	Control Register 1	0x0000_0490
SSPDR	0x0008	SSPDR is the data register and is 16-bits wide.	0x0000_0000
SSPSR	0x000C	Status Register. Reads from this register return SSP status.	0x0000_0003
SSPCPSR	0x0010	SSP Clock Pre-Scale Register. This register specifies the factor by which SSPCLK is to be divided in the Clock pre-scaler. The division factor has to be an even number from 2 to 254. The least significant bit of the programmed number is hard-coded to zero. If an odd number is written to this register, data read back from this register has the least significant bit as zero.	0x0000_0000
SSPIMSC	0x0014	The SSPIMSC register is the interrupt mask set or clear register. On a read, this register gives the current value of the mask on the relevant interrupt. A write of 1 to the particular bit sets the mask enabling the interrupt to be read. A write of 0 clears the corresponding mask	0x0000_0000
SSPRIS	0x0018	Raw Interrupt Status Register. On a read, this register gives the current raw status value of the corresponding interrupt prior to masking. A write has no effect	0x0000_0008
SSPMIS	0x001C	Masked Interrupt Status register. On a read, this register gives the current masked status value of the corresponding interrupt. A write has no effect.	0x0000_0000

Register	Offset	Description	Reset Value
SSPICR	0x0020	Interrupt Clear Register. On a write of 1, the corresponding interrupt is cleared. A write of 0 has no effect.	0x0000_0000
SSPDMACLR	0x0024	DMA Control Register	0x0000_0000
SSPPeriphID0	0x0FE0	Peripheral Identification Register Bits [7:0]	0x0000_1603
SSPPeriphID1	0x0FE4	Peripheral Identification Register Bits [15:8]	0x0000_1500
SSPPeriphID2	0x0FE8	Peripheral Identification Register Bits [23:16]	0x0000_0004
SSPPeriphID3	0x0FEC	Peripheral Identification Register Bits [31:24]	0x0000_0000
SSPCellID0	0x0FF0	PrimeCell Identification Register Bits [7:0]	0x0000_000D
SSPCellID1	0x0FF4	PrimeCell Identification Register Bits [15:8]	0x0000_00F0
SSPCellID2	0x0FF8	PrimeCell Identification Register Bits [23:16]	0x0000_0005
SSPCellID3	0x0FFC	PrimeCell Identification Register Bits [31:24]	0x0000_00B1

NOTE: If reserved or empty addresses in the register map are changed, S1SBP6A cannot guarantee normal operation.

4.2.10.2.1.1 SSPCR0

- Base Address: 0x4000_D000
- Address = Base Address + 0x0000, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
SCR	[15:8]	RW	Serial clock rate. The value SCR is used to generate the transmit and receive bit rate of the PrimeCell SSP. The bit rate is calculated using the following formula: FSSPCLK/{CPSDVR x (1+SCR)} where CPSDVSR is an even value from 2-254 programmed through the SSPCPSR register and SCR is a value from 0-255	0x0000_0000
SPH	[7]	RW	SSPCLKOUT phase (applicable to Motorola SPI frame format only). For more information, refer Chapter *4.2.10.1.7.2 Motorola SPI Frame Format*.	0x0000_0000
SPO	[6]	RW	SSPCLKOUT polarity (applicable to Motorola SPI frame format only). For more information, refer Motorola SPI frame format.	0x0000_0000
FRF	[5:4]	RW	* Frame format 00: Motorola SPI frame format 01: TI synchronous serial frame format 10: National Microwire frame format 11: Reserved, undefined operation	0x0000_0000
DSS	[3:0]	RW	* Data Size Select 0000: Reserved, undefined operation 0001: Reserved, undefined operation 0010: Reserved, undefined operation 0011: 4-bit data 0100: 5-bit data	0x0000_0000

Name	Bit	Type	Description	Reset Value
			0101: 6-bit data 0110: 7-bit data 0111: 8-bit data 1000: 9-bit data 1001: 10-bit data 1010: 11-bit data 1011: 12-bit data 1100: 13-bit data 1101: 14-bit data 1110: 15-bit data 1111: 16-bit data	

4.2.10.2.1.2 SSPCR1

- Base Address: 0x4000_D000
- Address = Base Address + 0x0004, Reset Value = 0x0000_0490

Name	Bit	Type	Description	Reset Value
TXIFLSELS	[12:10]	RW	* Selects TX FIFO Interrupt level 001: 1 (default) 010: 2 100: 4 Other: Reserved. Undefined operation.	0x0000_0001
TX_FIFO_CLEAR	[9]	WO	* Control TX FIFO clear 1'b1: FIFO Clear	0x0000_0000
RX_FIFO_CLEAR	[8]	WO	* Control RX FIFO clear 1'b1: FIFO Clear	0x0000_0000
MFSS	[7]	RW	* Control FSSOUT manually. FSSOUT is AND gated by MFSSOUT. 0: FSSOUT is Low. FSSOUT is manually controlled to be low. 1: FSSOUT is not manually controlled (default) * NOTE: In master mode, it operates on burst when MFSS is set 0 . In slave mode, it cannot operate on burst.	0x0000_0001
RXIFLSEL	[6:4]	RW	* Selects RX FIFO interrupt level 001: 1 (default) 010: 2 100: 4 Other: Reserved. Undefined operation.	0x0000_0001
SOD	[3]	RW	Slave-mode output disable. This bit is relevant only in the slave mode (MS=1). In multiple-slave systems, it is possible for a PrimeCell SSP master to broadcast a message to all slaves in the system while ensuring that only one slave drives data onto its serial output line. In such systems, the RXD lines from multiple slaves could be tied together.	0x0000_0000

Name	Bit	Type	Description	Reset Value
			* 'If the PrimeCell SSP slave is not supposed to drive the SSPTXD line, the SOD bit can be set to operate in such systems. 0: SSP can drive the SSPTXD output in slave mode 1: SSP must not drive the SSPTXD output in slave mode	
MS	[2]	RW	* Master or slave mode select. This bit can be modified only when the PrimeCell SSP is disabled (SSE=0) 0: Device configured as master (default) 1: Device configured as slave	0x0000_0000
SSE	[1]	RW	* Synchronous serial port enable 0: SSP operation disabled 1: SSP operation enabled	0x0000_0000
LBM	[0]	RW	* Loop back mode 0: Normal serial port operation enabled 1: Output of transmit serial shifter is connected to input of receive serial shifter internally	0x0000_0000

4.2.10.2.1.3 SSPDR

- Base Address: 0x4000_D000
- Address = Base Address + 0x0008, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
SSPDR	[15:0]	RW	SSPDR is the data register and is 16-bits wide. The entry in the receive FIFO (pointed to by the current FIFO read pointer) is accessed when SSPDR is read. As data values are removed by the PrimeCell SSP receive logic from the incoming data frame, they are placed into the entry in the receive FIFO (pointed to by the current FIFO write pointer). When SSPDR is written to the entry in the transmit FIFO pointed to by the write pointer, data values are removed from the transmit FIFO one value at a time by the transmit logic. It is loaded into the transmit serial shifter, then serially shifted out onto the SSPTXD pin at the programmed bit rate. When a data size of less than 16 bits is selected, the user must right-justify data written to the transmit FIFO. Unused bits at the top are ignored by transmit logic. Received data less than 16 bits is automatically right-justified in the receive buffer. * Transmit/Receive FIFO Read: Receive FIFO Write: Transmit FIFO	0x0000_0000

4.2.10.2.1.4 SSPSR

- Base Address: 0x4000_D000
- Address = Base Address + 0x000C, Reset Value = 0x0000_0003

Name	Bit	Type	Description	Reset Value
TX_FIFO_STATUS	[12:9]	R	TX FIFO Status (FIFO pointer value)	0x0000_0000
RX_FIFO_STATUS	[8:5]	R	RX FIFO Status (FIFO pointer value)	0x0000_0000
BSY	[4]	R	* PrimeCell SSP busy flag 0: SSP is idle 1: SSP is currently transmitting and/or receiving a frame or the transmit FIFO is not empty	0x0000_0000
RFF	[3]	R	* Receive FIFO full 0: Receive FIFO is not full 1: Receive FIFO is full	0x0000_0000
RNE	[2]	R	* Receive FIFO not empty 0: Receive FIFO is empty 1: Receive FIFO is not empty	0x0000_0000
TNF	[1]	R	* Transmit FIFO not full 0: Transmit FIFO is full 1: Transmit FIFO is not full	0x0000_0001
TFE	[0]	R	* Transmit FIFO empty 0: Transmit FIFO is not empty 1: Transmit FIFO is empty	0x0000_0001

4.2.10.2.1.5 SSPCPSR

- Base Address: 0x4000_D000
- Address = Base Address + 0x0010, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
SSPCPSR	[7:0]	RW	SSP Clock Pre-scale Register. This register specifies the factor by which SSPCLK is to be divided in the Clock pre-scaler. The division factor has to be an even number from 2 to 254. The least significant bit of the programmed number is hard-coded to zero. If an odd number is written to this register, data read back from this register has the least significant bit as zero.	0x0000_0000

4.2.10.2.1.6 SSPIMSC

- Base Address: 0x4000_D000
- Address = Base Address + 0x0014, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
TXIM	[3]	RW	* Transmit FIFO interrupt mask	0x0000_0000

Name	Bit	Type	Description	Reset Value
			0: Transmit FIFO half empty or less condition interrupt is masked 1: Transmit FIFO half empty or less condition interrupt is not masked	
RXIM	[2]	RW	* Receive FIFO interrupt mask 0: Receive FIFO half full or less condition interrupt is masked 1: Receive FIFO half full or less condition interrupt is not masked	0x0000_0000
RTIM	[1]	RW	* Receive timeout interrupt mask 0: Receive FIFO not empty and no read prior to timeout period interrupt is masked 1: Receive FIFO not empty and no read prior to timeout period interrupt is not masked	0x0000_0000
RORIM	[0]	RW	* Receive overrun interrupt mask 0: Receive FIFO write to when full condition interrupt is masked 1: Receive FIFO write when full condition interrupt is not masked	0x0000_0000

4.2.10.2.1.7 SSPRIS

- Base Address: 0x4000_D000
- Address = Base Address + 0x0018, Reset Value = 0x0000_0008

Name	Bit	Type	Description	Reset Value
TXRIS	[3]	R	Raw interrupt state of the SSPTXINTR interrupt prior to masking	0x0000_0001
RXRIS	[2]	R	Raw interrupt state of the SSPRXINTR interrupt prior to masking	0x0000_0000
RTRIS	[1]	R	Raw interrupt state of the SSPRTINTR interrupt prior to masking	0x0000_0000
RORRIS	[0]	R	Raw interrupt state of the SSPRORINTR interrupt prior to masking	0x0000_0000

4.2.10.2.1.8 SSPMIS

- Base Address: 0x4000_D000
- Address = Base Address + 0x001C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
TXMIS	[3]	R	Transmit FIFO masked interrupt state of the SSPTXINTR interrupt after masking	0x0000_0000
RXMIS	[2]	R	Receive FIFO masked interrupt state of the SSPRXINTR interrupt after masking	0x0000_0000
RTMIS	[1]	R	Receive timeout masked interrupt state of the SSPRTINTR	0x0000_0000

Name	Bit	Type	Description	Reset Value
			interrupt after masking	
RORMIS	[0]	R	Receive over run masked interrupt status of the SSPRORINTR interrupt after masking	0x0000_0000

4.2.10.2.1.9 SSPICR

- Base Address: 0x4000_D000
- Address = Base Address + 0x0020, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RTIC	[1]	W	Clears the SSPRTINTR interrupt	0x0000_0000
RORIC	[0]	W	Clears the SSPRORINTR interrupt	0x0000_0000

4.2.10.2.1.10 SSPDMACLR

- Base Address: 0x4000_D000
- Address = Base Address + 0x0024, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
TXDMAE	[1]	RW	Transmit DMA Enable. DMA for the transmit FIFO is enabled, if this bit is set to 1.	0x0000_0000
RXDMAE	[0]	RW	Receive DMA Enable. DMA for the receive FIFO is enabled, if this bit is set to 1.	0x0000_0000

4.2.10.2.1.11 SSPPeriphID0

- Base Address: 0x4000_D000
- Address = Base Address + 0x0FE0, Reset Value = 0x0000_1603

Name	Bit	Type	Description	Reset Value
SSPPeriphID0	[7:0]	R	Peripheral identification register bits [7:0]	0x0000_1603

4.2.10.2.1.12 SSPPeriphID1

- Base Address: 0x4000_D000
- Address = Base Address + 0x0FE4, Reset Value = 0x0000_1500

Name	Bit	Type	Description	Reset Value
SSPPeriphID1	[7:0]	R	Peripheral identification register bits [15:8]	0x0000_1500

4.2.10.2.1.13 SSPPeriphID2

- Base Address: 0x4000_D000

- Address = Base Address + 0x0FE8, Reset Value = 0x0000_0004

Name	Bit	Type	Description	Reset Value
SSPPeriphID2	[7:0]	R	Peripheral identification register bits [23:16]	0x0000_0004

4.2.10.2.1.14 SSPPeriphID3

- Base Address: 0x4000_D000
- Address = Base Address + 0x0FEC, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
SSPPeriphID3	[7:0]	R	Peripheral identification register bits [31:24]	0x0000_0000

4.2.10.2.1.15 SSPCellID0

- Base Address: 0x4000_D000
- Address = Base Address + 0x0FF0, Reset Value = 0x0000_000D

Name	Bit	Type	Description	Reset Value
SSPCellID0	[7:0]	R	PrimeCell identification register bits [7:0]	0x0000_000D

4.2.10.2.1.16 SSPCellID1

- Base Address: 0x4000_D000
- Address = Base Address + 0x0FF4, Reset Value = 0x0000_00F0

Name	Bit	Type	Description	Reset Value
SSPCellID1	[7:0]	R	PrimeCell identification register bits [15:8]	0x0000_00F0

4.2.10.2.1.17 SSPCellID2

- Base Address: 0x4000_D000
- Address = Base Address + 0x0FF8, Reset Value = 0x0000_0005

Name	Bit	Type	Description	Reset Value
SSPCellID2	[7:0]	R	PrimeCell identification register bits [23:16]	0x0000_0005

4.2.10.2.1.18 SSPCellID3

- Base Address: 0x4000_D000
- Address = Base Address + 0x0FFC, Reset Value = 0x0000_00B1

Name	Bit	Type	Description	Reset Value
SSPCellID3	[7:0]	R	PrimeCell identification register bits [31:24]	0x0000_00B1

Technical reference manual of SPI (PL022) can be found the link below.

http://infocenter.arm.com/help/topic/com.arm.doc.ddi0194g/DDI0194G_ssp_pl022_r1p3_trm.pdf

4.2.11 Advanced Encryption Standard

S1SBP6A utilizes Advanced Encryption Standard (AES) to secure the personal biometric information and body signals. The AES supports Electronic Code Block (ECB) and Cipher Block Chaining (CBC) modes. It also operates with 128-bit or 256-bit key sizes.

4.2.11.1 Register Description

This section describes the register map information and its associated registers.

4.2.11.1.1 Register Map Summary

- Base Address: 0x4002_3000

Register	Offset	Description	Reset Value
AESCON	0x0000	AES Control	0x0000_0000
AESSTATUS	0x0004	AES Status	0x0000_0002
AESINDATA1	0x0010	AES Input Data [31:0]	0x0000_0000
AESINDATA2	0x0014	AES Input Data [63:32]	0x0000_0000
AESINDATA3	0x0018	AES Input Data [95:64]	0x0000_0000
AESINDATA4	0x001C	AES Input Data [127:96]	0x0000_0000
AESOUTDATA1	0x0020	AES Output Data [31:0]	0x0000_0000
AESOUTDATA2	0x0024	AES Output Data [63:32]	0x0000_0000
AESOUTDATA3	0x0028	AES Output Data [95:64]	0x0000_0000
AESOUTDATA4	0x002C	AES Output Data [127:96]	0x0000_0000
AESIV1	0x0050	AES IV [31:0]	0x0000_0000
AESIV2	0x0054	AES IV [63:32]	0x0000_0000
AESIV3	0x0058	AES IV [95:64]	0x0000_0000
AESIV4	0x005C	AES IV [127:96]	0x0000_0000
AESKEY1	0x0080	AES Key [31:0]	0x0000_0000
AESKEY2	0x0084	AES Key [63:32]	0x0000_0000
AESKEY3	0x0088	AES Key [95:64]	0x0000_0000
AESKEY4	0x008C	AES Key [127:96]	0x0000_0000
AESKEY5	0x0090	AES Key [159:128]	0x0000_0000
AESKEY6	0x0094	AES Key [191:160]	0x0000_0000
AESKEY7	0x0098	AES Key [223:192]	0x0000_0000
AESKEY8	0x009C	AES Key [255:224]	0x0000_0000

NOTE: If reserved or empty addresses in the register map are changed, S1SBP6A cannot guarantee normal operation

4.2.11.1.1.1 AESCON

- Base Address: 0x4002_3000
- Address = Base Address + 0x0000, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD0	[31:6]	RW	*Reserved	0x0000_0000
AESKEY_SIZE	[5:4]	RW	*AES key size selection signal 00: 128 bit key 01: Reserved 10: 256 bit key 11: Reserved	0x0000_0000
RSVD1	[3:2]	RW	*Reserved	0x0000_0000
AES_CHAIN_MODE	[1]	RW	*AES chain mode selection signal 0: ECB mode 1: CBC mode	0x0000_0000
AES_OP	[0]	RW	*Encryption/decryption mode selection signal 0: Encryption 1: Decryption	0x0000_0000

4.2.11.1.1.2 AESSTATUS

- Base Address: 0x4002_3000
- Address = Base Address + 0x0004, Reset Value = 0x0000_0002

Name	Bit	Type	Description	Reset Value
RSVD0	[31:3]	RW	*Reserved	0x0000_0000
AES_BUSY	[2]	R	*AES busy signal 0: Idle 1: Busy	0x0000_0000
AES_IN_READY	[1]	R	*AES input ready signal 0: AES input buffer is not empty 1: AES input buffer is empty and the host is permitted to write the next block of data	0x0000_0001
AES_OUT_READY	[0]	RW	*AES output ready signal 0: AES output is not available 1: AES output is available	0x0000_0000

4.2.11.1.1.3 AESINDATA1

- Base Address: 0x4002_3000
- Address = Base Address + 0x0010, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
AESINDATA1	[31:0]	RW	*AES input data [31:0]	0x0000_0000

4.2.11.1.1.4 AESINDATA2

- Base Address: 0x4002_3000
- Address = Base Address + 0x0014, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
AESINDATA2	[31:0]	RW	*AES input data [63:32]	0x0000_0000

4.2.11.1.1.5 AESINDATA3

- Base Address: 0x4002_3000
- Address = Base Address + 0x0018, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
AESINDATA3	[31:0]	RW	*AES input data [95:64]	0x0000_0000

4.2.11.1.1.6 AESINDATA4

- Base Address: 0x4002_3000
- Address = Base Address + 0x001C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
AESINDATA4	[31:0]	RW	*AES input data [127:96]	0x0000_0000

4.2.11.1.1.7 AESOUTDATA1

- Base Address: 0x4002_3000
- Address = Base Address + 0x0020, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
AESOUTDATA1	[31:0]	R	*AES Output Data [31:0]	0x0000_0000

4.2.11.1.1.8 AESOUTDATA2

- Base Address: 0x4002_3000
- Address = Base Address + 0x0024, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
AESOUTDATA2	[31:0]	R	*AES Output Data [63:32]	0x0000_0000

4.2.11.1.1.9 AESOUTDATA3

- Base Address: 0x4002_3000
- Address = Base Address + 0x0028, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
AESOUTDATA3	[31:0]	R	*AES Output Data [95:64]	0x0000_0000

4.2.11.1.1.10 AESOUTDATA4

- Base Address: 0x4002_3000
- Address = Base Address + 0x002C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
AESOUTDATA4	[31:0]	R	*AES Output Data [127:96]	0x0000_0000

4.2.11.1.1.11 AESIV1

- Base Address: 0x4002_3000
- Address = Base Address + 0x0050, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
AESIV1	[31:0]	RW	*AES IV [31:0]	0x0000_0000

4.2.11.1.1.12 AESIV2

- Base Address: 0x4002_3000
- Address = Base Address + 0x0054, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
AESIV2	[31:0]	RW	*AES IV [63:32]	0x0000_0000

4.2.11.1.1.13 AESIV3

- Base Address: 0x4002_3000
- Address = Base Address + 0x0058, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
AESIV3	[31:0]	RW	*AES IV [95:64]	0x0000_0000

4.2.11.1.1.14 AESIV4

- Base Address: 0x4002_3000
- Address = Base Address + 0x005C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
AESIV4	[31:0]	RW	*AES IV [127:96]	0x0000_0000

4.2.11.1.1.15 AESKEY1

- Base Address: 0x4002_3000
- Address = Base Address + 0x0080, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
AESKEY1	[31:0]	W	*AES Key [31:0]	0x0000_0000

4.2.11.1.1.16 AESKEY2

- Base Address: 0x4002_3000
- Address = Base Address + 0x0084, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
AESKEY2	[31:0]	W	*AES Key [63:32]	0x0000_0000

4.2.11.1.1.17 AESKEY3

- Base Address: 0x4002_3000
- Address = Base Address + 0x0088, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
AESKEY3	[31:0]	W	*AES Key [95:64]	0x0000_0000

4.2.11.1.1.18 AESKEY4

- Base Address: 0x4002_3000
- Address = Base Address + 0x008C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
AESKEY4	[31:0]	W	*AES Key [127:96]	0x0000_0000

4.2.11.1.1.19 AESKEY5

- Base Address: 0x4002_3000
- Address = Base Address + 0x0090, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
AESKEY5	[31:0]	W	*AES Key [159:128]	0x0000_0000

4.2.11.1.1.20 AESKEY6

- Base Address: 0x4002_3000
- Address = Base Address + 0x0094, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
AESKEY6	[31:0]	W	*AES Key [191:160]	0x0000_0000

4.2.11.1.1.21 AESKEY7

- Base Address: 0x4002_3000
- Address = Base Address + 0x0098, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
AESKEY7	[31:0]	W	*AES Key [223:192]	0x0000_0000

4.2.11.1.1.22 AESKEY8

- Base Address: 0x4002_3000
- Address = Base Address + 0x009C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
AESKEY8	[31:0]	W	*AES Key [255:224]	0x0000_0000

4.2.12 Digital True Random Number Generator

Digital True Random Number Generator (DTRNG) system generates random numbers from thermal noise of a chip. The generated random numbers are non-deterministic sequence of bits and unpredictable. It consists of Clock Divider, TRNG, Post Processor, and TRNG FIFO. The clock frequency of TRNG block should be less than 0.1 MHz for stable operation. You can adjust the TRNG clock frequency. The random bits from TRNG block can have a bias which means the random bits can have more ones than zeros or vice versa. So, DTRNG system includes Post Processor as a bias compensator. Post Processor supports four different bias compensation methods which are Bypass, Linear Feedback Shift Register (LFSR), Von Neumann (VN), and XOR. Random bit from Post Processor is gathered at TRNG FIFO sequentially. After FIFO is filled up, you can read 32-bit random data from FIFO at a time. *Figure 4-45* illustrates the block diagram of DTRNG system.

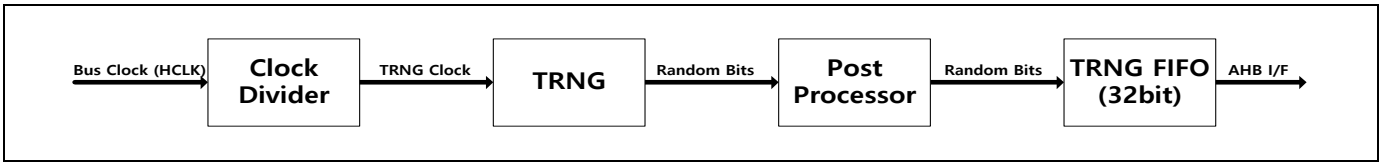


Figure 4-45 Block Diagram of DTRNG System

Table 4-7 describes the latencies of post processor.

Table 4-7 Latencies of Post Processor

Post Processor Mode	Latency in TRNG Clocks	32-bit Example in TRNG Clocks
Bypass	No latency	32
LFSR	31	63 (31 + 32) for initial generation 32 for next generations
VN	Approximately 4 times	Average 128 (32 × 4)
XOR	2 times	64 (32 × 2)

Figure 4-46 illustrates the operation flow of DTRNG.

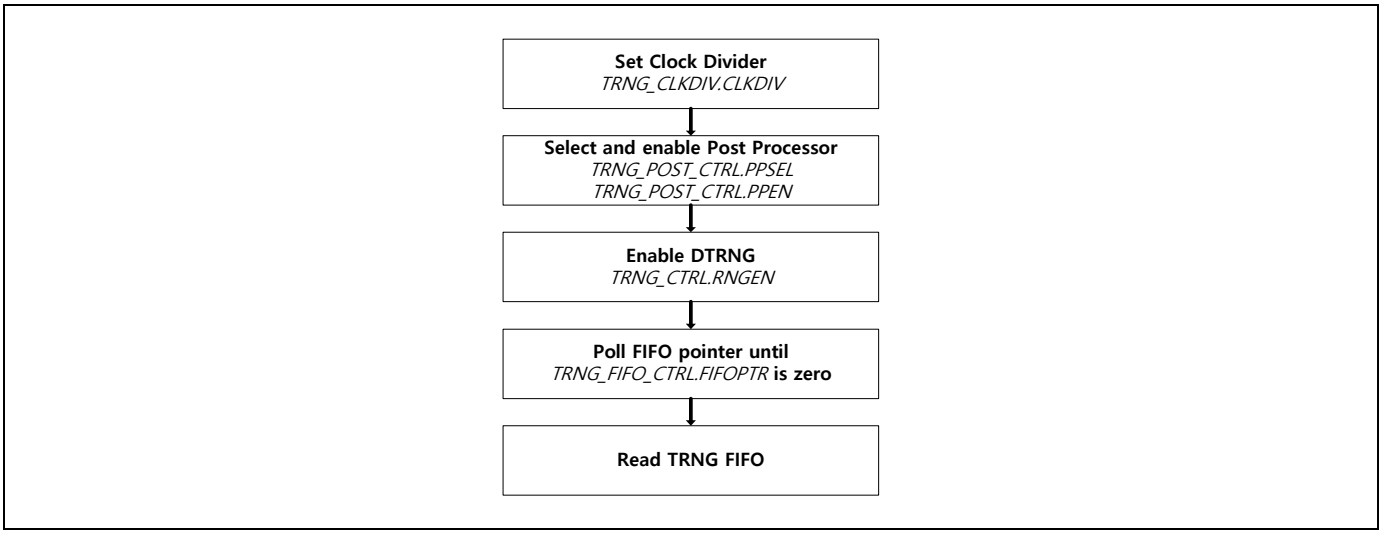


Figure 4-46 Operation Flow of DTRNG System

4.2.12.1 Register Description

This section describes the register map information and its associated registers.

4.2.12.1.1 Register Map Summary

- Base Address: 0x4002_3000

Register	Offset	Description	Reset Value
TRNG_CLKDIV	0x0000	TRNG Clock Divider	0x0000_00C8
TRNG_CTRL	0x0004	TRNG Control	0x0000_0000
TRNG_POST_CTRL	0x0008	TRNG Post Processor Control	0x0000_0000
TRNG_FIFO_CTRL	0x000C	TRNG FIFO Control	0x0000_0000
TRNG_FIFO_0	0x0010	TRNG FIFO Control	0x0000_0000

NOTE: If reserved or empty addresses in the register map are changed, S1SBP6A cannot guarantee normal operation.

4.2.12.1.1.1 TRNG_CLKDIV

- Base Address: 0x4002_3000
- Address = Base Address + 0x0000, Reset Value = 0x0000_00C8

Name	Bit	Type	Description	Reset Value
RSVD0	[31:16]	RW	*Reserved	0x0000_0000
CLKDIV	[15:0]	RW	*The frequency of system clock is divided by CLKDIV to generate frequency of slow clock. If this value is 10, then the period of slow clock in TRNG is ten times longer than the period of system clock (AHB clock). The clock divider must be an even number. So, CLKDIV [0] bit is reserved to protect dividing odd number.	0x0000_00C8

4.2.12.1.1.2 TRNG_CTRL

- Base Address: 0x4002_3000
- Address = Base Address + 0x0004, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RNGEN	[31]	RW	*Random number generator enable bit. This bit enables TRNG. After 32 bits are filled in FIFO, this bit is automatically cleared.	0x0000_0000
RSVD0	[30:0]	RW	*Reserved	0x0000_0000

4.2.12.1.1.3 TRNG_POST_CTRL

- Base Address: 0x4002_3000
- Address = Base Address + 0x0008, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
PPEN	[31]	RW	*Post processor enable bit. This bit enables the post processor. 0: Disables the post processor. The random bit bypasses the post processor in any value of PPSEL. 1: Enables the post processor.	0x0000_0000
RSVD0	[30:2]	RW	*Reserved	0x0000_0000
PPSEL	[1:0]	RW	*Post processor selector bit. 00: The random bit bypasses the post processor. 01: The random bit is processed by LFSR post processor. 10: The random bit is processed by Von Neumann (VN) post processor. 11: The random bit is processed by XOR post processor	0x0000_0000

4.2.12.1.1.4 TRNG_FIFO_CTRL

- Base Address: 0x4002_3000
- Address = Base Address + 0x000C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD0	[31:9]	R	*Reserved	0x0000_0000
FIFOPTR	[5:0]	R	*FIFO pointer bits. This is a pointer to a flip-flop in TRNG FIFO to store next random bit. If this value is bigger than zero, FIFO[FifoPtr-1] is filled with a random bit. Then, FifoPtr is decremented by 1 until it becomes zero. 1~32: A random bit is generated and stored in FIFO[FifoPtr-1] and FifoPtr is decremented by 1.	0x0000_0000

4.2.12.1.1.5 TRNG_FIFO_0

- Base Address: 0x4002_3000
- Address = Base Address + 0x0010, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
FIFO_0	[31:0]	R	*TRNG FIFO [31:0]. LSB is the first random bit received.	0x0000_0000

4.2.13 Real Time Clock

Real Time Clock (RTC) unit operates using the backup battery when the system power is off. When the power is off, the backup battery can store the time by Second, Minute, Hour, Date of the week, Day, Month, and Year data. The RTC unit works with an external clock source.

4.2.13.1 Feature

RTC supports Binary Coded Decimal (BCD) Number, that is, second, minute, hour, day of the week, day, month and year. RTC also supports Leap Year Generator. The Leap Year Generator determines the last day of each month out of 28, 29, 30, or 31 days. This is calculated based on the data from BCD DAY, BCD MON, and BCD YEAR. This block considers leap year while deciding on the last day of a month. The BCDYEAR register is 7-bit wide. It can represent maximum three BCD digits. The implicit number of thousands place is 20. Therefore, it can represent years from 2000 to 2099.

4.2.13.2 Functional Description

4.2.13.2.1 Architecture

RTC is consists of Clock divider, Control Registers, Reset Register, Leap Year Generator, and Alarm Generator. Clock divider is a core module which makes 1 Hz clock from 32.768 kHz and calculates time. Alarm Generator is a module which makes control signal for RTC and generates tick and wake-up signal. Control Registers and Reset Register are interface modules with APB bus. *Figure 4-47* illustrates the block diagram of RTC.

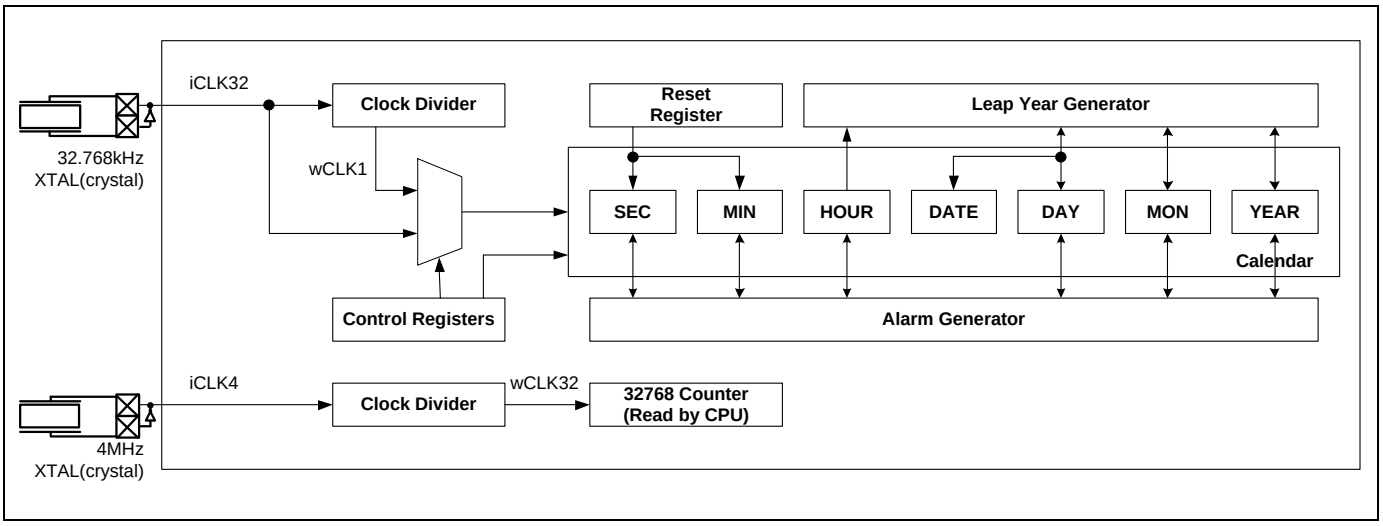


Figure 4-47 Block Diagram of RTC

4.2.13.2.1.1 Leap Year Generator

The leap year generator determines the last day of each month out of 28, 29, 30, or 31 days. This is calculated based on the data from BCDDAY, BCDMON, and BCDYEAR. This block considers leap year while deciding on the last day of a month. The BCDYEAR register is 7-bit wide. It can represent maximum three BCD digits. The implicit

number of thousands place is 20. Therefore, it can represent years from 400 × n to 400 × n + 999 (n = 0, 1, 2, 3, 4, 5, and so on).

4.2.13.2.1.2 Alarm Generator

The RTC generates alarm interrupt at a specific time during the power-off mode or normal operation mode. The RTC alarm register determines the alarm Enable/Disable status and the condition of the alarm time setting.

4.2.13.3 Register Description

This section describes the register map information and its associated registers.

4.2.13.3.1 Register Map Summary

- Base Address: 0x4001_9000

Register	Offset	Description	Reset Value
CALENDAR_MODE	0x0020	CALENDAR_MODE	0x0000_0000
GEN_COUNT_CLR	0x0024	GEN_COUNT_CLR	0x0000_0000
LOAD_COUNT_SIG	0x0028	LOAD_COUNT_SIG	0x0000_0000
LOAD_COUNT_VALUE0	0x002C	LOAD_COUNT_VALUE0	0x0000_0000
LOAD_COUNT_VALUE1	0x0030	LOAD_COUNT_VALUE1	0x0000_0000
LOAD_COUNT_VALUE2	0x0034	LOAD_COUNT_VALUE2	0x0000_0000
LOAD_COUNT_VALUE3	0x0038	LOAD_COUNT_VALUE3	0x0000_0000
LOAD_COUNT_VALUE4	0x003C	LOAD_COUNT_VALUE4	0x0000_0000
LOAD_COUNT_VALUE5	0x0040	LOAD_COUNT_VALUE5	0x0000_0000
CALENDAR_COUNT_VALUE0	0x0044	CALENDAR_COUNT_VALUE0	0x0000_0000
CALENDAR_COUNT_VALUE1	0x0048	CALENDAR_COUNT_VALUE1	0x0000_0000
CALENDAR_COUNT_VALUE2	0x004C	CALENDAR_COUNT_VALUE2	0x0000_0000
CALENDAR_COUNT_VALUE3	0x0050	CALENDAR_COUNT_VALUE3	0x0000_0000
CALENDAR_COUNT_VALUE4	0x0054	CALENDAR_COUNT_VALUE4	0x0000_0000
CALENDAR_COUNT_VALUE5	0x0058	CALENDAR_COUNT_VALUE5	0x0000_0000
CALENDAR_TIME_STAMP	0x005C	CALENDAR_TIME_STAMP	0x0000_0000
INT_ENABLE_CPU	0x0060	INT_ENABLE_CPU	0x0000_0000
INT_CLEAR_CPU	0x0064	INT_CLEAR_CPU	0x0000_0000
SYNC_INT_TIME0	0x006C	SYNC_INT_TIME0	0x0000_0000
SYNC_INT_TIME1	0x0070	SYNC_INT_TIME1	0x0000_0000
INT_STATUS_CPU	0x0074	INT_STATUS_CPU	0x0000_0000
ALARM_ENABLE	0x0078	ALARM_ENABLE	0x0000_0000
ALARM_COUNT_VALUE0	0x007C	ALARM_COUNT_VALUE0	0x0000_0000
ALARM_COUNT_VALUE1	0x0080	ALARM_COUNT_VALUE1	0x0000_0000
ALARM_COUNT_VALUE2	0x0084	ALARM_COUNT_VALUE2	0x0000_0000
ALARM_COUNT_VALUE3	0x0088	ALARM_COUNT_VALUE3	0x0000_0000
ALARM_COUNT_VALUE4	0x008C	ALARM_COUNT_VALUE4	0x0000_0000
ALARM_COUNT_VALUE5	0x0090	ALARM_COUNT_VALUE5	0x0000_0000
GENERAL_COUNT0	0x0094	GENERAL_COUNT0	0x0000_0000

Register	Offset	Description	Reset Value
GENERAL_COUNT1	0x0098	GENERAL_COUNT1	0x0000_0000
STOP_COUNT_ENABLE	0x009C	STOP_COUNT_ENABLE	0x0000_0000
STOP_COUNT_CLEAR	0x00A0	STOP_COUNT_CLEAR	0x0000_0000
STOP_COUNT_TIME_STAMP0	0x00A4	STOP_COUNT_TIME_STAMP0	0x0000_0000
STOP_COUNT_TIME_STAMP1	0x00A8	STOP_COUNT_TIME_STAMP1	0x0000_0000
STOP_COUNT_TIME_STAMP2	0x00AC	STOP_COUNT_TIME_STAMP2	0x0000_0000
STOP_COUNT_TIME_STAMP3	0x00B0	STOP_COUNT_TIME_STAMP3	0x0000_0000
AUTO_COUNT_CLR	0x00B4	AUTO_COUNT_CLR	0x0000_0000
STOP_COUNT_LOAD0	0x00B8	STOP_COUNT_LOAD0	0x0000_0000
STOP_COUNT_LOAD1	0x00BC	STOP_COUNT_LOAD1	0x0000_0000
STOP_COUNT_LOAD2	0x00C0	STOP_COUNT_LOAD2	0x0000_0000
STOP_COUNT_LOAD3	0x00C4	STOP_COUNT_LOAD3	0x0000_0000
GENERAL_COUNT_SNAP_SHOT_COMMAND	0x00C8	GENERAL_COUNT_SNAP_SHOT_COMMAND	0x0000_0000
STOP_COUNT_SNAP_SHOT_COMMAND	0x00CC	STOP_COUNT_SNAP_SHOT_COMMAND	0x0000_0000

NOTE: If reserved or empty addresses in the register map are changed, S1SBP6A cannot guarantee normal operation.

4.2.13.3.1.1 CALENDAR_MODE

- Base Address: 0x4001_9000
- Address = Base Address + 0x0020, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
HOUR_MODE	[1]	RW	1'b0: 12h mode 1'b1: 24h mode	0x0000_0000
ENABLE	[0]	RW	1'b0: Calendar mode disable 1'b1: Calendar mode enable	0x0000_0000

4.2.13.3.1.2 GEN_COUNT_CLR

- Base Address: 0x4001_9000
- Address = Base Address + 0x0024, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
GEN_COUNT_CLR	[0]	RW	* Clear signal for 32k general counter.	0x0000_0000

4.2.13.3.1.3 LOAD_COUNT_SIG

- Base Address: 0x4001_9000
- Address = Base Address + 0x0028, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
LOAD_COUNT_SIG	[6:0]	RW	* Calendar Count Load signal. [6] : YEAR value load [5] : MON value load [4] : DATE value load [3] : DAY value load [2] : HOUR value load [1] : MIN value load [0] : SEC value load	0x0000_0000

4.2.13.3.1.4 LOAD_COUNT_VALUE0

- Base Address: 0x4001_9000
- Address = Base Address + 0x002C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD0	[7:6]	RW	Reserved	0x0000_0000
SEC	[5:0]	RW	Second value	0x0000_0000

4.2.13.3.1.5 LOAD_COUNT_VALUE1

- Base Address: 0x4001_9000
- Address = Base Address + 0x0030, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD0	[7:6]	RW	Reserved	0x0000_0000
MIN	[5:0]	RW	Minute value	0x0000_0000

4.2.13.3.1.6 LOAD_COUNT_VALUE2

- Base Address: 0x4001_9000
- Address = Base Address + 0x0034, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD0	[7:5]	RW	Reserved	0x0000_0000
HOUR	[4:0]	RW	Hour value	0x0000_0000

4.2.13.3.1.7 LOAD_COUNT_VALUE3

- Base Address: 0x4001_9000
- Address = Base Address + 0x0038, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
DAY	[4:0]	RW	Day value	0x0000_0000

4.2.13.3.1.8 LOAD_COUNT_VALUE4

- Base Address: 0x4001_9000
- Address = Base Address + 0x003C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
MON	[7:4]	RW	Month value	0x0000_0000
RSVD0	[3]	RW	Reserved	0x0000_0000
DATE	[2:0]	RW	Date value	0x0000_0000

4.2.13.3.1.9 LOAD_COUNT_VALUE5

- Base Address: 0x4001_9000
- Address = Base Address + 0x0040, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
YEAR	[6:0]	RW	Year value	0x0000_0000

4.2.13.3.1.10 CALENDAR_COUNT_VALUE0

- Base Address: 0x4001_9000
- Address = Base Address + 0x0044, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
SEC	[6:0]	R	Second value	0x0000_0000

4.2.13.3.1.11 CALENDAR_COUNT_VALUE1

- Base Address: 0x4001_9000
- Address = Base Address + 0x0048, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
MIN	[6:0]	R	Minute value	0x0000_0000

4.2.13.3.1.12 CALENDAR_COUNT_VALUE2

- Base Address: 0x4001_9000
- Address = Base Address + 0x004C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
HOUR	[5:0]	R	Hour value	0x0000_0000

4.2.13.3.1.13 CALENDAR_COUNT_VALUE3

- Base Address: 0x4001_9000
- Address = Base Address + 0x0050, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
DAY	[5:0]	R	Day value	0x0000_0000

4.2.13.3.1.14 CALENDAR_COUNT_VALUE4

- Base Address: 0x4001_9000
- Address = Base Address + 0x0054, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
MON	[7:3]	R	Month value	0x0000_0000
DATE	[2:0]	R	Date value	0x0000_0000

4.2.13.3.1.15 CALENDAR_COUNT_VALUE5

- Base Address: 0x4001_9000
- Address = Base Address + 0x0058, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
AMPM	[7]	R	AM/PM value	0x0000_0000
YEAR	[6:0]	R	Year value	0x0000_0000

4.2.13.3.1.16 CALENDAR_TIME_STAMP

- Base Address: 0x4001_9000
- Address = Base Address + 0x005C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CALENDAR_TIME_STAMP	[0]	RW	Time stamp command for Calendar value	0x0000_0000

4.2.13.3.1.17 INT_ENABLE_CPU

- Base Address: 0x4001_9000
- Address = Base Address + 0x0060, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
INT_ENABLE_CPU	[2:0]	RW	Interrupt enable for CPU_INTC	0x0000_0000

4.2.13.3.1.18 INT_CLEAR_CPU

- Base Address: 0x4001_9000
- Address = Base Address + 0x0064, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
INT_CLEAR_CPU	[2:0]	RW	Interrupt clear for CPU_INTC	0x0000_0000

4.2.13.3.1.19 SYNC_INT_TIME0

- Base Address: 0x4001_9000
- Address = Base Address + 0x006C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
SYNC_INT_TIME0	[7:0]	RW	SYNC Interrupt enable and generation count selection [15]:Enable [14:0]:32.768 kHz Clock count	0x0000_0000

4.2.13.3.1.20 SYNC_INT_TIME1

- Base Address: 0x4001_9000
- Address = Base Address + 0x0070, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
SYNC_INT_TIME1	[7:0]	RW	SYNC Interrupt enable and generation count selection [15]:Enable [14:0]:32.768 kHz Clock count	0x0000_0000

4.2.13.3.1.21 INT_STATUS_CPU

- Base Address: 0x4001_9000
- Address = Base Address + 0x0074, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
INT_STATUS_CPU	[2:0]	R	Interrupt status for CPU_INTC	0x0000_0000

4.2.13.3.1.22 ALARM_ENABLE

- Base Address: 0x4001_9000
- Address = Base Address + 0x0078, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ALARM_ENABLE	[6:0]	RW	Alarm match enable [6] : YEAR alarm enable [5] : MON alarm enable [4] : DATE alarm enable [3] : DAY alarm enable [2] : HOUR alarm enable [1] : MIN alarm enable [0] : SEC alarm enable	0x0000_0000

4.2.13.3.1.23 ALARM_COUNT_VALUE0

- Base Address: 0x4001_9000
- Address = Base Address + 0x007C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
SEC	[6:0]	RW	Second value	0x0000_0000

4.2.13.3.1.24 ALARM_COUNT_VALUE1

- Base Address: 0x4001_9000
- Address = Base Address + 0x0080, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
MIN	[6:0]	RW	Minute value	0x0000_0000

4.2.13.3.1.25 ALARM_COUNT_VALUE2

- Base Address: 0x4001_9000
- Address = Base Address + 0x0084, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
HOUR	[5:0]	RW	Hour value	0x0000_0000

4.2.13.3.1.26 ALARM_COUNT_VALUE3

- Base Address: 0x4001_9000
- Address = Base Address + 0x0088, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
DAY	[5:0]	RW	Day value	0x0000_0000

4.2.13.3.1.27 ALARM_COUNT_VALUE4

- Base Address: 0x4001_9000
- Address = Base Address + 0x008C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
MON	[7:3]	RW	Month value	0x0000_0000
DATE	[2:0]	RW	Date value	0x0000_0000

4.2.13.3.1.28 ALARM_COUNT_VALUE5

- Base Address: 0x4001_9000
- Address = Base Address + 0x0090, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
YEAR	[7:0]	RW	Year value	0x0000_0000

4.2.13.3.1.29 GENERAL_COUNT0

- Base Address: 0x4001_9000
- Address = Base Address + 0x0094, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
GENERAL_COUNT0	[7:0]	R	32 kHz general count snap shot	0x0000_0000

4.2.13.3.1.30 GENERAL_COUNT1

- Base Address: 0x4001_9000
- Address = Base Address + 0x0098, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
GENERAL_COUNT1	[6:0]	R	32 kHz general count snap shot	0x0000_0000

4.2.13.3.1.31 STOP_COUNT_ENABLE

- Base Address: 0x4001_9000
- Address = Base Address + 0x009C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
STOP_COUNT_ENABLE	[0]	RW	Stop counter enable 1'b1 : Enable 1'b0 : Disable	0x0000_0000

4.2.13.3.1.32 STOP_COUNT_CLEAR

- Base Address: 0x4001_9000
- Address = Base Address + 0x00A0, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
STOP_COUNT_CLEAR	[0]	RW	Clear signal for stop counter (32.768 kHz 32 bit counter)	0x0000_0000

4.2.13.3.1.33 STOP_COUNT_TIME_STAMP0

- Base Address: 0x4001_9000
- Address = Base Address + 0x00A4, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
STOP_COUNT_TIME_STAMP0	[7:0]	R	Stop counter snap shot value	0x0000_0000

4.2.13.3.1.34 STOP_COUNT_TIME_STAMP1

- Base Address: 0x4001_9000
- Address = Base Address + 0x00A8, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
STOP_COUNT_TIME_STAMP1	[7:0]	R	Stop counter snap shot value	0x0000_0000

4.2.13.3.1.35 STOP_COUNT_TIME_STAMP2

- Base Address: 0x4001_9000
- Address = Base Address + 0x00AC, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
STOP_COUNT_TIME_STAMP2	[7:0]	R	Stop counter snap shot value	0x0000_0000

4.2.13.3.1.36 STOP_COUNT_TIME_STAMP3

- Base Address: 0x4001_9000
- Address = Base Address + 0x00B0, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
STOP_COUNT_TIME_STAMP3	[7:0]	R	Stop counter snap shot value	0x0000_0000

4.2.13.3.1.37 AUTO_COUNT_CLR

- Base Address: 0x4001_9000
- Address = Base Address + 0x00B4, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
AUTO_COUNT_CLR	[0]	RW	Auto wrap up control enable of 32.768 kHz 32 bit counter when counter reaches STOP_COUNT_LOAD value. 1'b1 : Auto wrapup enable, 1'b0 : Auto wrapup disable	0x0000_0000

4.2.13.3.1.38 STOP_COUNT_LOAD0

- Base Address: 0x4001_9000
- Address = Base Address + 0x00B8, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
STOP_COUNT_LOAD0	[7:0]	RW	Stop counter match count (32.768 kHz 32 bit counter)	0x0000_0000

4.2.13.3.1.39 STOP_COUNT_LOAD1

- Base Address: 0x4001_9000
- Address = Base Address + 0x00BC, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
STOP_COUNT_LOAD1	[7:0]	RW	Stop counter match count (32.768 kHz 32 bit counter)	0x0000_0000

4.2.13.3.1.40 STOP_COUNT_LOAD2

- Base Address: 0x4001_9000
- Address = Base Address + 0x00C0, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
STOP_COUNT_LOAD2	[7:0]	RW	Stop counter match count (32.768 kHz 32 bit counter)	0x0000_0000

4.2.13.3.1.41 STOP_COUNT_LOAD3

- Base Address: 0x4001_9000
- Address = Base Address + 0x00C4, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
STOP_COUNT_LOAD3	[7:0]	RW	Stop counter match count (32.768 kHz 32 bit counter)	0x0000_0000

4.2.13.3.1.42 GENERAL_COUNT_SNAP_SHOT_COMMAND

- Base Address: 0x4001_9000
- Address = Base Address + 0x00C8, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
GENERAL_COUNT_SNAP_SHOT_COMMAND	[0]	RW	32 kHz general count snap shot command	0x0000_0000

4.2.13.3.1.43 STOP_COUNT_SNAP_SHOT_COMMAND

- Base Address: 0x4001_9000
- Address = Base Address + 0x00CC, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
STOP_COUNT_SNAP_SHOT_COMMAND	[0]	RW	Stop counter snap shot command	0x0000_0000

4.2.14 Flash Controller

Flash controller consists of an internal 2 MB Flash and 2 KB Cache. Flash controller is connected with two AHB buses, system bus for flash IP, and multiplexed Instruction/Data-code bus for flash controller.

Flash controller supports the following features:

- 2X/4X prefetch mode for high-speed operation
- Error Correction Code (ECC) function for improvement in flash cell reliability Cache for improvement in NOR flash memory performance
- *Figure 4-48* illustrates the flash controller connection.

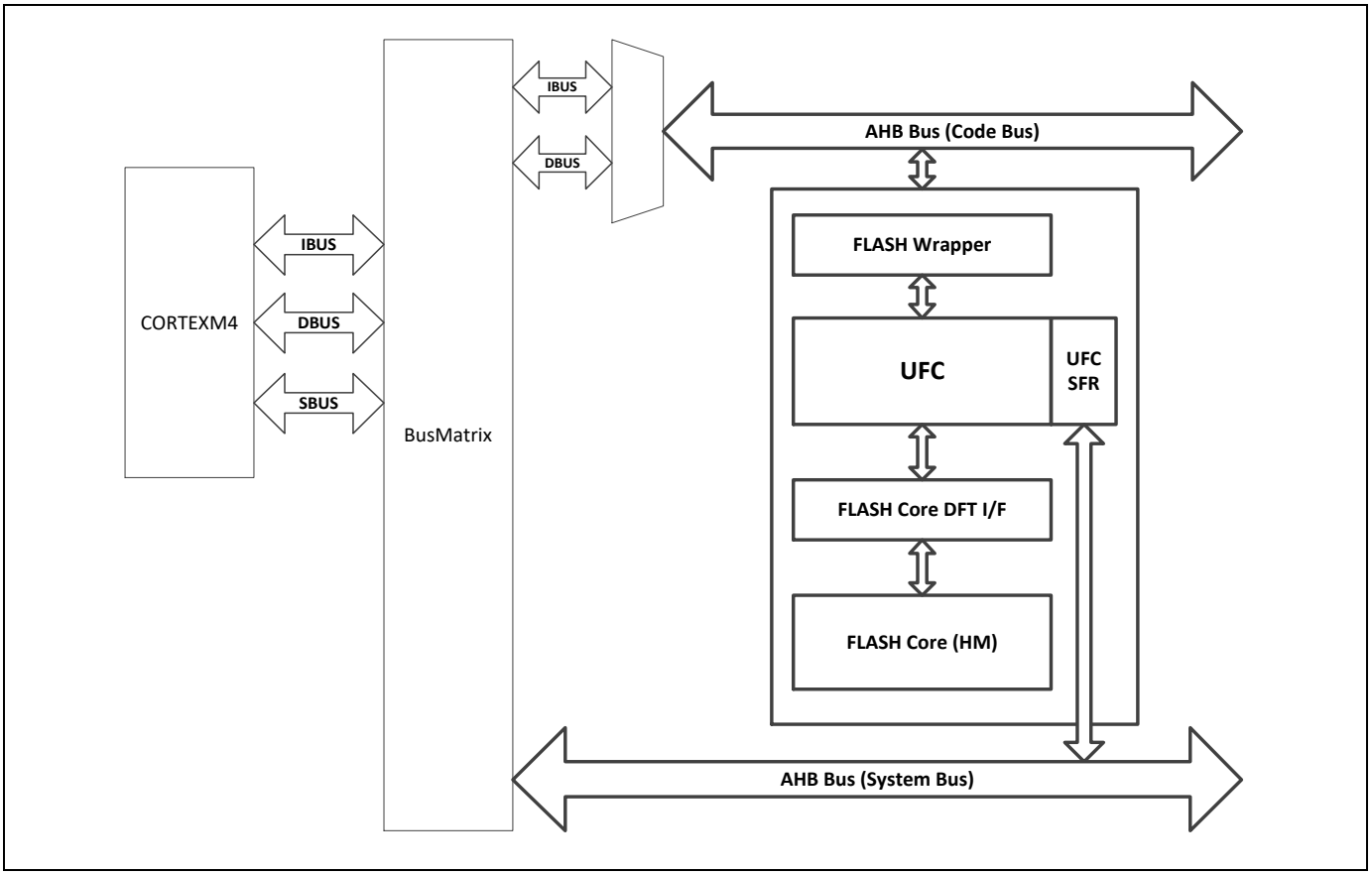


Figure 4-48 Flash Controller Connection

Figure 4-49 illustrates the block diagram of Flash controller.

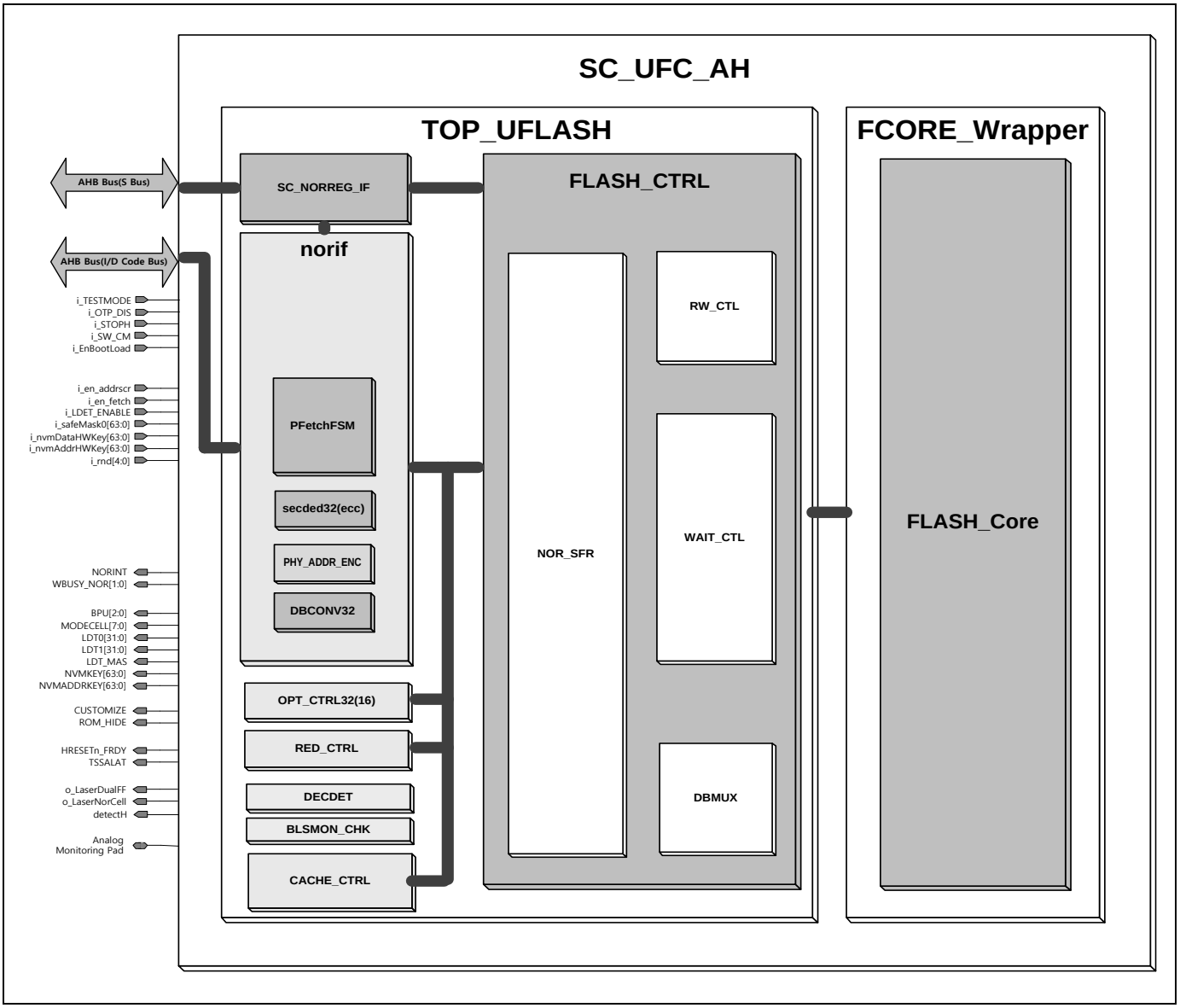


Figure 4-49 Block Diagram of Flash Controller

4.2.14.1 Functional Description

4.2.14.1.1 Flash Memory Array

Flash memory consists of the following main array and option cells.

- IF block is 3ea pages and includes security and code protection information.
- DCT/LDT/PROT/RED is of 1ea page size (1 page = 512 Bytes)
- DCT block includes option (trim) of flash core
- LDT block includes user option information
- PROT0~8 include user protection information
- RED includes repair information of row redundancy
- There is 1ea Row Redundancy Array per Matrix and 1ea Row Redundancy Array consists of 4ea pages.

Figure 4-50 illustrates the flash memory array.

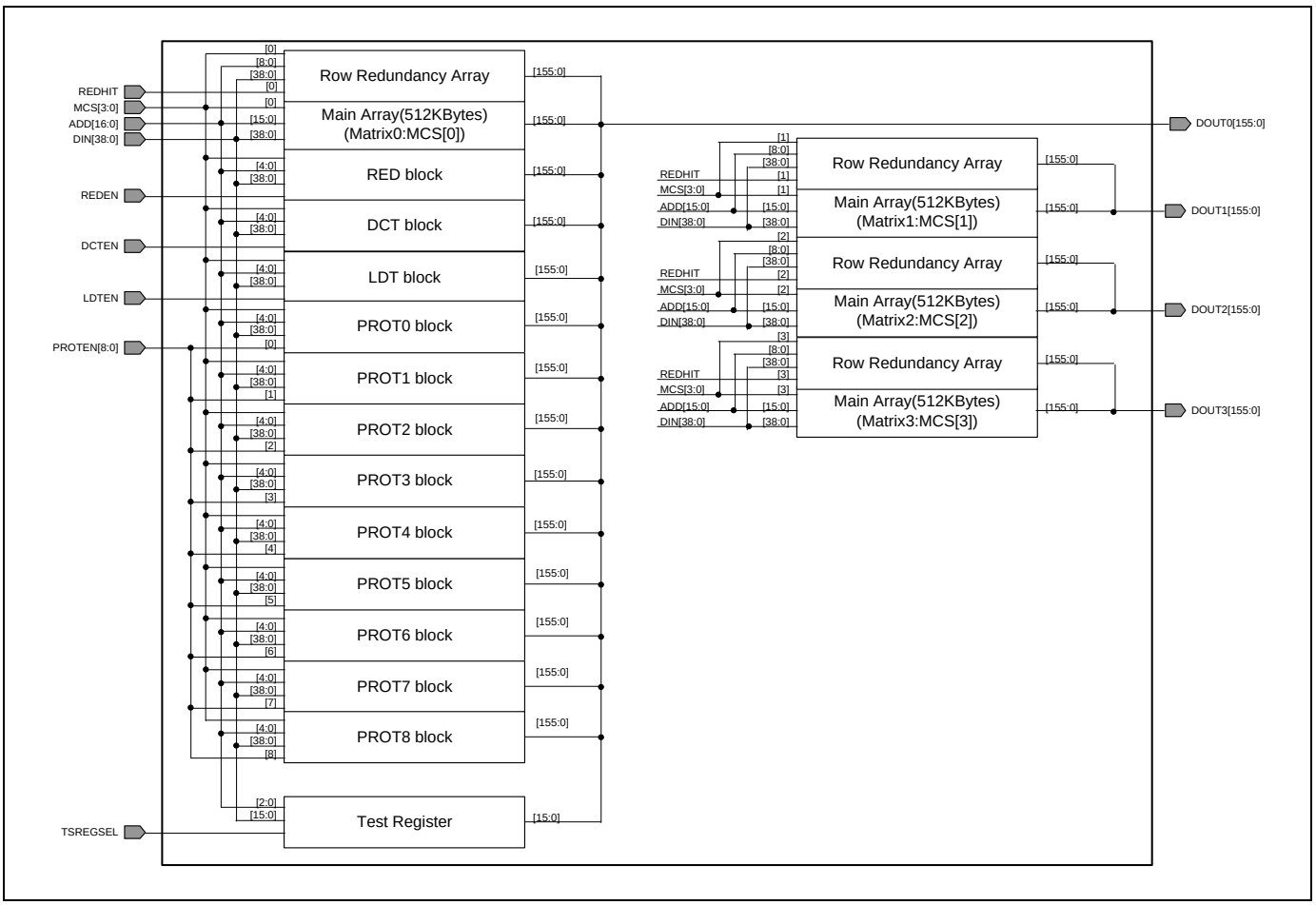


Figure 4-50 Flash Memory Array

4.2.14.1.2 Description of Optional Area Access

Figure 4-51 illustrates the option block configuration.

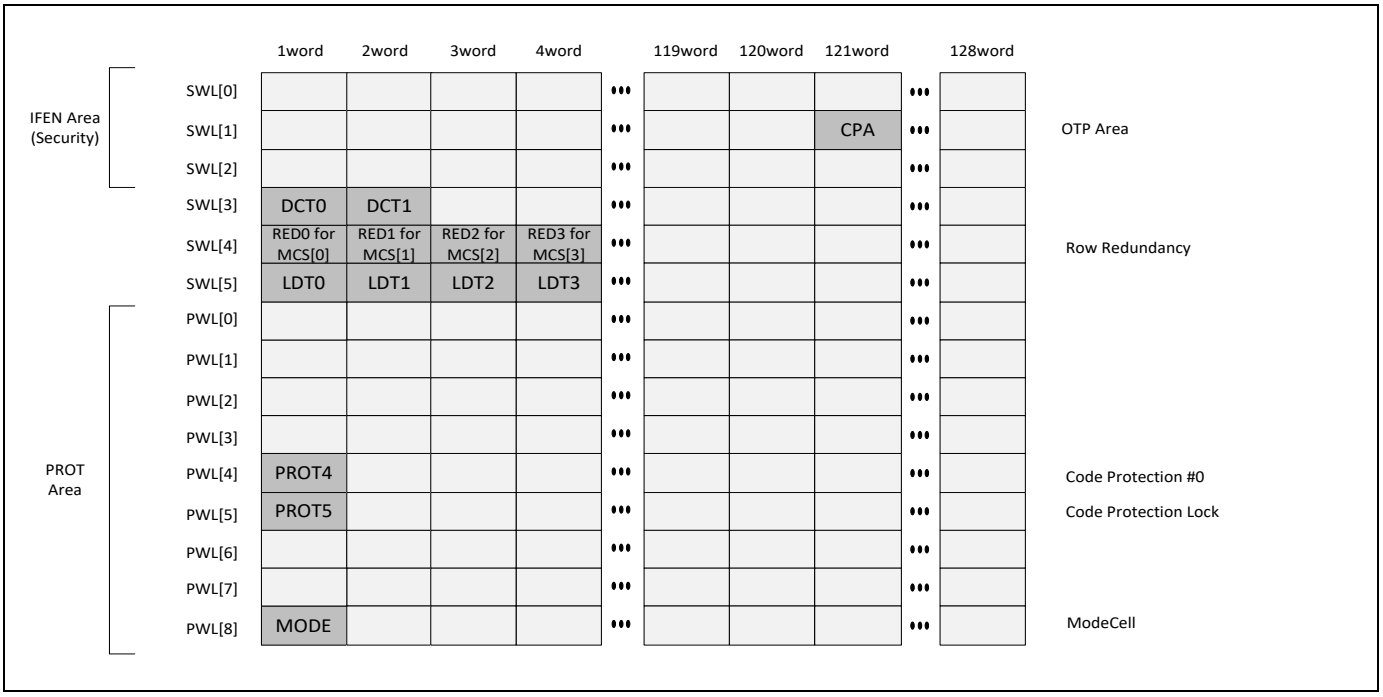


Figure 4-51 Option Block Configuration

4.2.14.1.2.1 Description of Optional Area Access

4.2.14.1.2.1.1 Information Area (Security Area) Access

IF(security) Area	Test Mode	User Mode	Note
Security Area #0	Read/ERS/PGM	Read only	–
Security Area #1	Read/ERS/PGM	Skipped ERS&PGM	OTP
Security Area #2	Read/ERS/PGM	Read/ERS/PGM	–

4.2.14.1.2.1.2 Loading Data Information in Boot Configuration (OTP AREA)

Usage	CPA[15:0]	Note
Address	SEC_BASE + OPT_adCPA	–
Valid bit	DIN[15:0]	–

NOTE:

1. Code Protection Area (CPA) can be assigned by sector address unit (Address[27:12])
2. OPT_adCPA = 0x3E0
3. Protection area = 0x00 ~ {~CPA[15:0], 12'hFFF}
4. CPA = ~ DIN[31:0] (for example, 0xFFFFFFFD → Protection area = 0x00 ~ 0x2FFF)
5. Save the CPA value to Password area whose offset address is 0x08-0x09 in security area.

4.2.14.1.2.1.3 PROT/LDT Area Access

Mode	PROT Area			LDT Area		
	Select Signal	Valid Data Bit	Access Type	Select Signal	Valid Data Bit	Access Type
Test Mode	PROTEN[7:0]	DIN[3:0]	Read/ERS/PGM	LDTEN	DIN[31:0]	Read/ERS/PGM
User Mode	PROTEN[7:0]	DIN[3:0]	Read/ERS/PGM	N/A	N/A	N/A

NOTE:

1. If Lock bit is set, PROT area cannot be erased/programmed.
2. Selection bit of PROTEN[7:0] / LDTEN / DCTEN / MODEEN is not available at a time
3. LDTEN = LDTCON[0]
4. LDT = ~ DIN[31:0] (for example, 0x55555555 → MEM@LDT=0xAAAAAAAA)

4.2.14.1.2.1.4 DCT Area Access

Mode	DCT Area		
	Select signal	Valid Data Bit	Access Type
Test Mode	DCTEN	DIN[31:0]	Read/ERS/PGM
User Mode	N/A	N/A	N/A

NOTE: DCTEN = LDTCON[2]

4.2.14.1.2.1.5 MODE Area Access

Mode	MODE Area		
	Select signal	Valid Data Bit	Access Type
Test Mode	MODEEN	DIN[26:16], DIN[11:0]	Read/ERS/PGM
User Mode	N/A	N/A	N/A

NOTE:

1. MODEEN = LDTCON[4]
2. MODE= ~ DIN[26:0] (for example, 0x55555555 → MEM@MODE=0xAAAAAAAA)
3. DIN[26:16] of MODE Area is assigned option of UFC.
4. DIN[26:16]={data wait extended opt[26:25], erase verify guard time[24:23],ecc disable[22], hslatchen[21], fecccon access[20], variable data access of literal pool area[19], prefetch disable[18], ecc mode[17:16]}

4.2.14.1.2.1.6 Redundancy Area Access

Mode	RED Area		
	Select Signal	Valid Data Bit	Access Type
Test Mode	REDEN	DIN[8:0]	Read/ERS/PGM
User Mode	N/A	N/A	N/A

NOTE: REDEN = LDTCON[1]

4.2.14.1.3 Supported Operations

The flash controller supports write and erase operation. Write operation sets the selected bits to 0. Erase operation sets the selected bits to 1.

User can check the FRWCON register before every write or erase operation. When FRWCON is not 0x0000, other function is processing the flash operation. User has to wait until the FRWCON is set to 0x0000.

4.2.14.1.3.1 Write Operation

Write operations must be performed on erased WU, that is, the value of the WU must be 0xFFFFFFFF before write operation. *Figure 4-52* illustrates the write operation.

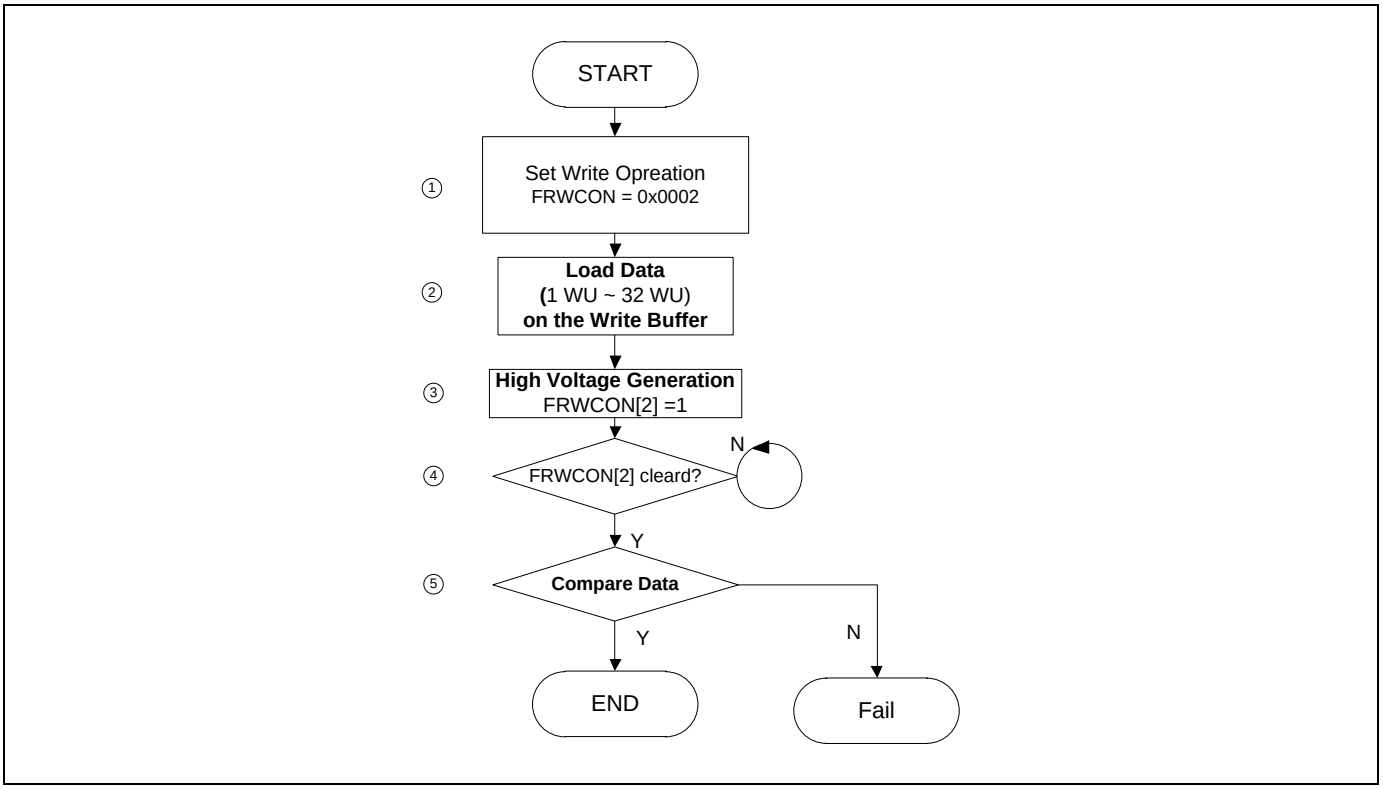


Figure 4-52 Write Operation

Legend	Description
1	Select write operation: FRWCON = 0x0002.
2	Store RAM data to the targeted WU. At this time, the data is loaded on the write buffer from RAM.
3	Activate high voltage operation FRWCON[2] = 1.
4	Wait for high voltage to end until FRWCON = 0x0000.
5	It is recommended to Read all data and compare with the expected value.

4.2.14.1.3.2 Erase Operation

Figure 4-53 illustrates the erase operation.

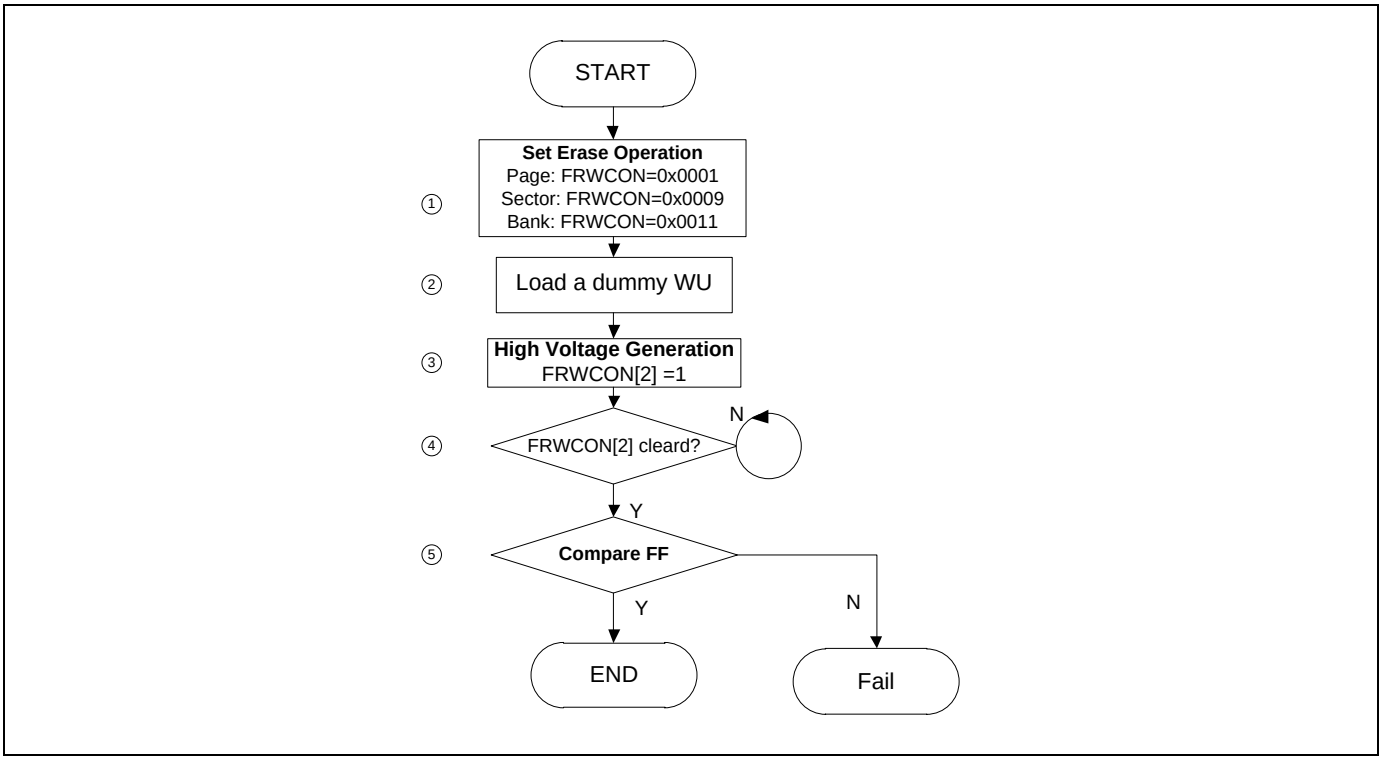


Figure 4-53 Erase Operation

Legend	Description
1	Select erase operation and the desired erase unit (FRWCON = (sector)0x0009 / (bank)0x0011 / (page) 0x0001)
2	Store dummy value to any WU within the target area: At this time, a dummy WU is loaded on the write buffer.
3	Activate high voltage operation FRWCON[2] = 1.
4	Wait for high voltage to end until FRWCON = 0x0000.
5	It is recommended to read all data and compare with 0xFFFFFFFF.

4.2.14.1.3.3 Option Cell Program Operation

Figure 4-54 illustrates the option cell program operation.

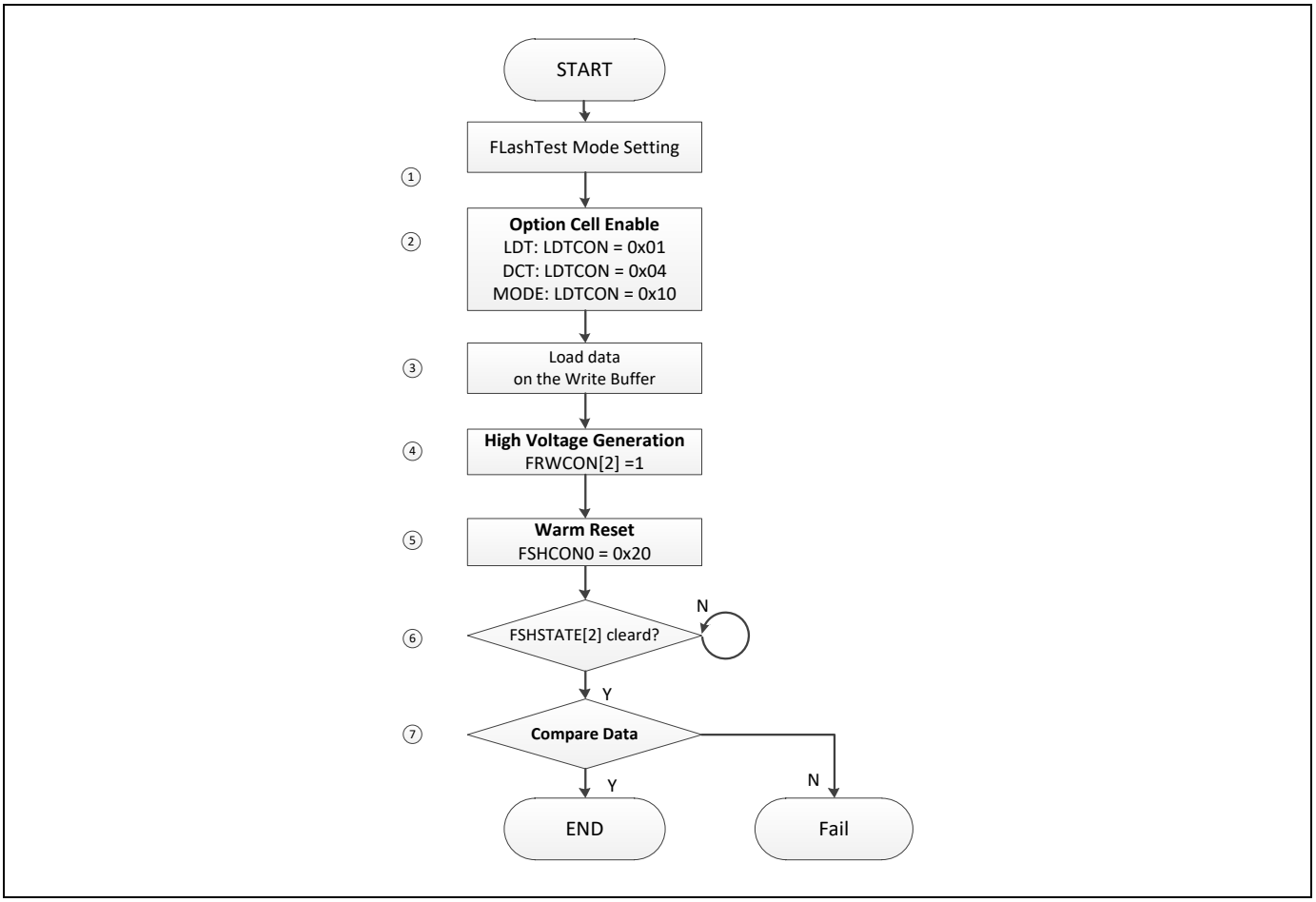


Figure 4-54 Option Cell Program Operation

4.2.14.1.3.4 Interrupt control

After Erase/Write operation, the interrupt source to the MCU core is generated.

4.2.14.2 Flash IP Specifications

Table 4-8 describes the flash IP specifications.

Table 4-8 Flash IP Specifications

Product		Reset Value
Organization	Memory Density	2 MB (4 Matrix)
	Program Page Buffer Size	512 Byte
	Data Input	39 bit (7 bit for ECC)
	Data Output	156 bit (28 bit for ECC), X4
Power	VDDF	1.1 V -5% +10%
	VDDHF	1.62 V ~ 5.5 V
Operating Temperature		-25 °C ~ 85 °C
Endurance		500 Kcycle
Data Retention		20 years
	Erase Unit	Page (512 Byte) Sector (2K Byte) Mat (512 KByte) Chip (2 MByte)
Read Access Time	Endurance (< 1K cycle for Code)	30 ns
	Endurance (< 500K cycle for Data)	80 ns

4.2.14.3 Register Description

This section describes the register map information and its associated registers.

4.2.14.3.1 Register Map Summary

- Base Address: 0x4002_5000

Register	Offset	Description	Reset Value
FRWCON0	0x0000	FRWCON0 Register	0x0000_0000
FSHSTAT	0x0004	Flash Status Register	0x0000_0000
PROTCON	0x0010	OPRSEL OR BLSCON	0x0000_0000
PROTMON	0x0014	BLSMON in ARM	0x0000_030F
DCYCRDCON	0x0020	DCYCREAD Control Register	0x0000_0004
LDTCON	0x0030	LDTCON Register for TESTMODE ONLY	0x0000_0000
FSHCON0	0x0034	Flash Test Register #1	0x0000_0000
FECCCON	0x0038	Flash Test Register #2	0x0000_0000
FECCFADR	0x003C	ECC Fault Address	0x0000_0000
DCT0	0x0040	DCT0 Option Register	0xFFFF_FFFF
DCT1	0x0044	DCT1 Option Register	0xFFFF_FFFF
LDT0	0x0050	LDT0 Option Register	0x0000_0000
LDT1	0x0054	LDT1 Option Register	0x0000_0000
LDT2	0x0058	LDT2 Option Register	0x0000_0000
LDT3	0x005C	LDT3 Option Register	0x0000_0000
MODE	0x0060	MODECELL Option Register	0x0000_0000
CPA0	0x0064	CPA0 Option Register	0x0000_0000
RED0	0x0090	MAT0 RED Address Value	0x0000_0000
RED0_MBIT	0x0094	MAT0 RED Address Master Value	0x0000_0000
RED1	0x0098	MAT1 RED Address Value	0x0000_0000
RED1_MBIT	0x009C	MAT1 RED Address Master Value	0x0000_0000
RED2	0x00A0	MAT2 RED Address Value	0x0000_0000
RED2_MBIT	0x00A4	MAT2 RED Address Master Value	0x0000_0000
RED3	0x00A8	MAT3 RED Address Value	0x0000_0000
RED3_MBIT	0x00AC	MAT3 RED Address Master Value	0x0000_0000

NOTE: If reserved or empty addresses in the register map are changed, S1SBP6A cannot guarantee normal operation.

4.2.14.3.1.1 FRWCON0

- Base Address: 0x4002_5000
- Address = Base Address + 0x0000, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD0	[31:16]	R	Reserved	0x0000_0000
ECC_Fail_Flag	[15]	RW	ECC fail flag 0: ECC data correct 1: If DOUT_ECC[6:0]!=7'hFF, ECC Fail flag is set. When you want to check this bit again, you must set this bit to 0.	0x0000_0000
ECC_DATA	[14:8]	R	ECC data bits (= DCOUT_ECC[6:0])	0x0000_0000
RSVD1	[7:5]	RW	Reserved (always 0)	0x0000_0000
EraseModeselection	[4:3]	RW	Erase mode selection 00: Page Erase mode(512 bytes) 01: Sector Erase mode (2 Kbytes) 10: Mat Erase mode (Mat Erase) 11: Forbidden	0x0000_0000
ProgramActivation	[2]	RW	Program activation bit 0: No operation 1: High voltage generation	0x0000_0000
EraseWriteSelection	[1:0]	RW	Erase and write selection bits 00: No operation 01: Erase 10: Write 11: Forbidden	0x0000_0000

4.2.14.3.1.2 FSHSTAT

- Base Address: 0x4002_5000
- Address = Base Address + 0x0004, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD0	[31:4]	R	Reserved	0x0000_0000
FSHSTAT	[3:0]	RW	Flash Status bits 0000: No error 0001: Option read completion after cold reset 0010: Option read completion after warm reset (Testmode only) 0011: No page buffer load 0100: More than 2 word page load 0101: No pgm or ers mode set 0110: Write while write 0111: frwcon undefined set 1000: Dual read mode detection (prefetch and dcycread)	0x0000_0000

4.2.14.3.1.3 PROTCON

- Base Address: 0x4002_5000
- Address = Base Address + 0x0010, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD0	[31:12]	R	Reserved	0x0000_0000
CodeProtectionLock	[11:10]	W	2'b01 : Lock Code Protection enable bits 2'b 10: Unlocking code protection enable bit 2'b 01: Locking Code Protection enable bit If you want to permanently lock code protection attribute in Flash area (PROTMON[5]= 0), you must follow the following sequence:. 1) Set these bits to 01 : Erase 2) Set these bits to 01 : Program	0x0000_0000
CodeProtection0	[9:8]	W	2'b10 : If you want to use the flash area as writeable. 2'b 10: MAT0 Writable 2'b 01: MAT0 Write Protection If user want not to be writable flash area(PROTMON[4]= 0), user must follow the below sequences. 1) Set these bits to 01 : Erase 2) Set these bits to 01 : Program	0x0000_0000
RSVD1	[7:0]	R	Reserved (always 0)	0x0000_0000

4.2.14.3.1.4 PROTMON

- Base Address: 0x4002_5000
- Address = Base Address + 0x0014, Reset Value = 0x0000_030F

Name	Bit	Type	Description	Reset Value
RSVD0	[31:11]	R	Reserved	0x0000_0000
CP_LOCK	[9]	R	Code Protection Lock Monitoring bit 0 : Flash code protection is locked 1: Flash code protection is unlocked	0x0000_0001
CP_SET	[8]	R	Flash write enable bit 0: Flash write protection (read only) 1: Flash writable	0x0000_0001
RSVD1	[7:4]	R	Reserved	0x0000_0000
RSVD2	[3:0]	R	Reserved	0x0000_000F

4.2.14.3.1.5 DCYCRDCON

- Base Address: 0x4002_5000
- Address = Base Address + 0x0020, Reset Value = 0x0000_0004

Name	Bit	Type	Description	Reset Value
RSVD0	[31:16]	R	Reserved	0x0000_0000
RSVD1	[15:12]	RW	Reserved	0x0000_0000
Bank0DataWait	[11:8]	RW	NOR Flash Bank0 Data read wait cycle 0000: No wait 0001: 1 wait 0010: 2 wait 0011: 3 wait 0100: 4 wait 0101: 5 wait 0110: 6 wait 0111: 7 wait 1000: 8 wait 1001: 9 wait Others : Forbidden	0x0000_0000
RSVD2	[7:6]	RW	Reserved	0x0000_0000
Bank0CodeWait	[5:4]	RW	NOR Flash Bank0 Code read wait cycle 00: No wait 01: 1 wait 10: 2 wait (2x prefetch mode is not supported) 11: 3 wait (2x prefetch mode is not supported)	0x0000_0000
CAC_FLUSH	[3]	RW	NOR Flash Cache Flush bit 0: Remain Cache 1: Cache Flush	0x0000_0000
CAC_EN	[2]	RW	NOR Flash Branch Cache enable bit 0: Cache disabled 1: Cache enabled	0x0000_0001
Noeffect	[1]	RW	NOR Flash 4X Prefetch control bit 0: Prefetch disabled 1: Prefetch enabled	0x0000_0000
_2XPrefetchenable	[0]	RW	NOR Flash 2X Prefetch control bit 0: Prefetch disabled 1: Prefetch enabled	0x0000_0000

4.2.14.3.1.6 LDTCON

- Base Address: 0x4002_5000
- Address = Base Address + 0x0030, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD0	[31:5]	R	Reserved	0x0000_0000
ModeCell	[4]	RW	ModeCell Selection bit 0: No action 1: Modecell enable	0x0000_0000
RSVD1	[3]	RW	Reserved	0x0000_0000
DCT Option	[2]	RW	DCT Option Selection bit 0: No action 1: DCT option enable	0x0000_0000
RED Option	[1]	RW	Redundancy option selection bit 0: No action 1: Redundancy option enable	0x0000_0000
LDT0 Option	[0]	RW	LDT0 Option selection bit 0: No action 1: LDT0 option enable	0x0000_0000

4.2.14.3.1.7 FSHCON0

- Base Address: 0x4002_5000
- Address = Base Address + 0x0034, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD0	[31:11]	R	Reserved	0x0000_0000
ChipEraseEnable	[10]	RW	Total chip erase enable bit 0: Chip Erase disable 1: Chip Erase enable	0x0000_0000
Reserved	[9]	RW	Reserved	0x0000_0000
Write_data_inverting_selection	[8]	RW	Write data inverting selection bit 0: Inverting disable 1: Inverting enable	0x0000_0000
SALAT_measure_bit_for_trim	[7]	RW	SALAT measure bit for trim 0: SALAT inactive 1: SALAT active	0x0000_0000
HSATCHcontrol	[6]	RW	HSLATCH enable bit for EDS 0: HSLATHC disable (HSLATCH → always 1) 1: HSLATHC enable (HSLATCH → code: 1, data:0)	0x0000_0000
Option_value_update	[5]	RW	Option value update enable 0: Disable 1: Enable	0x0000_0000
Reserved1	[4]	R	Reserved	0x0000_0000
Read_DB_path_delay_measure	[3]	RW	Read data but path delay measure enable 0: No action 1: Read data bus delay measure enable	0x0000_0000
Test_Register_access	[2]	RW	Test Register access enable 0: Test register access disable 1: Test register access enable	0x0000_0000
UserModeTestSelection	[1]	RW	User mode set enable 0: No action 1: User mode test enable	0x0000_0000
IFEN	[0]	RW	IFEN Enable bit 0: No action 1: IFEN enable	0x0000_0000

4.2.14.3.1.8 FECCCON

- Base Address: 0x4002_5000
- Address = Base Address + 0x0038, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD0	[31:15]	R	Reserved	0x0000_0000
ECCWritedata	[14:8]	RW	ECC write data bits	0x0000_0000
RSVD1	[7]	R	Reserved	0x0000_0000
ECC_fault_clear	[6]	RW	ECC fault clear bit (auto clear at next clock)	0x0000_0000
ECC_fault_type	[5:4]	R	ECC fault type monitoring bits	0x0000_0000
RSVD2	[3:2]	R	Reserved	0x0000_0000
ECCMain_data_access_type_selection	[1:0]	RW	ECC/Main Data access type selection bits	0x0000_0000

4.2.14.3.1.9 FECCFADR

- Base Address: 0x4002_5000
- Address = Base Address + 0x003C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ECC_fault_address	[31:0]	R	ECC fault address	0x0000_0000

4.2.14.3.1.10 DCT0

- Base Address: 0x4002_5000
- Address = Base Address + 0x0040, Reset Value = 0x0FFF_FFFF

Name	Bit	Type	Description	Reset Value
DCT0	[31:0]	RW	DCT0[31:0] option value	0xFFFF_FFFF

4.2.14.3.1.11 DCT1

- Base Address: 0x4002_5000
- Address = Base Address + 0x0044, Reset Value = 0x0FFF_FFFF

Name	Bit	Type	Description	Reset Value
DCT1	[31:0]	RW	DCT1[31:0] option value	0xFFFF_FFFF

4.2.14.3.1.12 LDT0

- Base Address: 0x4002_5000
- Address = Base Address + 0x0050, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
LDT0	[31:0]	RW	LDT0[31:0] option value	0x0000_0000

4.2.14.3.1.13 LDT1

- Base Address: 0x4002_5000
- Address = Base Address + 0x0054, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
LDT1	[31:0]	RW	LDT1[31:0] option value	0x0000_0000

4.2.14.3.1.14 LDT2

- Base Address: 0x4002_5000
- Address = Base Address + 0x0058, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
LDT2	[31:0]	RW	LDT2[31:0] option value	0x0000_0000

4.2.14.3.1.15 LDT3

- Base Address: 0x4002_5000
- Address = Base Address + 0x005C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
LDT3	[31:0]	RW	LDT3[31:0] option value	0x0000_0000

4.2.14.3.1.16 MODE

- Base Address: 0x4002_5000
- Address = Base Address + 0x0060, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD0	[31:29]	R	Reserved	0x0000_0000
UFC_OPTCELL10	[28]	R	ECC fail flag auto clear option 0: ECC fail flag auto clear disable 1: ECC fail flag auto clear enable	0x0000_0000
UFC_OPTCELL9	[27]	R	Performance Enhanced option in case of sequential read after idle 0: disable 1: enable	0x0000_0000
UFC_OPTCELL8	[26:25]	R	Data wait extended option 00: default_wait (2w/3w) 01: default_wait + 1 (3w/4w) 10: default_wait + 2 (4w/5w) 11: default_wait + 3 (5w/6w)	0x0000_0000
UFC_OPTCELL7	[24:23]	R	Erase verify read guard time decrease option 00: ref_vfycnt 01: ref_vfycnt -1 10: ref_vfycnt -2 11: ref_vfycnt -3	0x0000_0000
UFC_OPTCELL6	[22]	R	ECC Function disable option 0: ECC function enable 1: ECC function disable	0x0000_0000
UFC_OPTCELL5	[21]	R	HSLATCH attribute enable option 0: Always code 1: On/Off by Code/Data access	0x0000_0000
UFC_OPTCELL4	[20]	R	FECCCON register access mode select option 0: No accessible in Umode 1: Accessible in Umode	0x0000_0000
UFC_OPTCELL3	[19]	R	Data wait operating mode set option 0: Wait by setting en_wait 1: Wait by HPROT[0]	0x0000_0000
UFC_OPTCELL2	[18]	R	Prefetch disable option	0x0000_0000
UFC_OPTCELL1	[17]	R	Cache disable option bit 0: Cache enable 1: Cache disable	0x0000_0000
UFC_OPTCELL0	[16]	R	Post ecc mode enable 0: Disable 1: Post ecc mode enable	0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD1	[15:9]	R	Reserved	0x0000_0000
LDT_MCELL	[11:8]	R	Option value for LDT master	0x0000_0000
MODECELL	[7:0]	R	MODECELL[7:0] option value	0x0000_0000

4.2.14.3.1.17 CPA0

- Base Address: 0x4002_5000
- Address = Base Address + 0x0064, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD0	[31:16]	R	Reserved	0x0000_0000
CPA0	[15:0]	R	CPA0 Option value (Code Protection #0)	0x0000_0000

4.2.14.3.1.18 RED0

- Base Address: 0x4002_5000
- Address = Base Address + 0x0090, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD0	[31:8]	R	Reserved	0x0000_0000
RED0	[7:0]	RW	MAT0 RED Address value(= {Repair Addr[17:10]}) • Repair_Addr[17:10]: (MAT0 offset address(Mat0 PhysicalAddress)	0x0000_0000

4.2.14.3.1.19 RED0_MBIT

- Base Address: 0x4002_5000
- Address = Base Address + 0x0094, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD0	[31:1]	R	Reserved	0x0000_0000
RED0_MBIT	[0]	RW	MAT0 RED Address Master value(RED0_MBIT) • RED_MBIT = 1: Repaired, 0: No repair	0x0000_0000

4.2.14.3.1.20 RED1

- Base Address: 0x4002_5000
- Address = Base Address + 0x0098, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD0	[31:8]	R	Reserved	0x0000_0000
RED1	[7:0]	RW	MAT1 RED Address value(={Repair Addr[17:10]}) • Repair_Addr[17:10]: (MAT1 offset address (Mat1 PhysicalAddress)	0x0000_0000

4.2.14.3.1.21 RED1_MBIT

- Base Address: 0x4002_5000
- Address = Base Address + 0x009C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD0	[31:1]	R	Reserved	0x0000_0000
RED1_MBIT	[0]	RW	MAT1 RED Address Master value(RED1_MBIT) • RED_MBIT=1: Repaired, 0: No repair	0x0000_0000

4.2.14.3.1.22 RED2

- Base Address: 0x4002_5000
- Address = Base Address + 0x00A0, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD0	[31:8]	R	Reserved	0x0000_0000
RED2	[7:0]	RW	MAT2 RED Address value(={Repair Addr[17:10]}) • Repair_Addr[17:10]: (MAT2 offset address(Mat2 PhysicalAddress)	0x0000_0000

4.2.14.3.1.23 RED2_MBIT

- Base Address: 0x4002_5000
- Address = Base Address + 0x00A4, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD0	[31:1]	R	Reserved	0x0000_0000
RED2_MBIT	[0]	RW	MAT2 RED Address Master value(RED2_MBIT) • RED_MBIT=1: Repaired, 0: No repair	0x0000_0000

4.2.14.3.1.24 RED3

- Base Address: 0x4002_5000
- Address = Base Address + 0x00A8, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD0	[31:8]	R	Reserved	0x0000_0000
RED3	[7:0]	RW	MAT3 RED Address value(={Repair Addr[17:10]}) • Repair_Addr[17:10]: (MAT3 offset address(Mat3 PhysicalAddress)	0x0000_0000

4.2.14.3.1.25 RED3_MBIT

- Base Address: 0x4002_5000
- Address = Base Address + 0x00A8, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD0	[31:1]	R	Reserved	0x0000_0000
RED3_MBIT	[0]	RW	MAT3 RED Address Master value(RED3_MBIT) • RED_MBIT=1: Repaired, 0: No repair	0x0000_0000

4.2.15 Serial Flash Interface

Serial Flash Interface (SFI) enables communications with external serial flash with SPI protocol.

SFI supports the following features:

- Single/Quad mode
- Maximum 256-byte burst write
- AHB slave interface Serial flash interface commands
- *Figure 4-55* illustrates the block diagram of SFI.

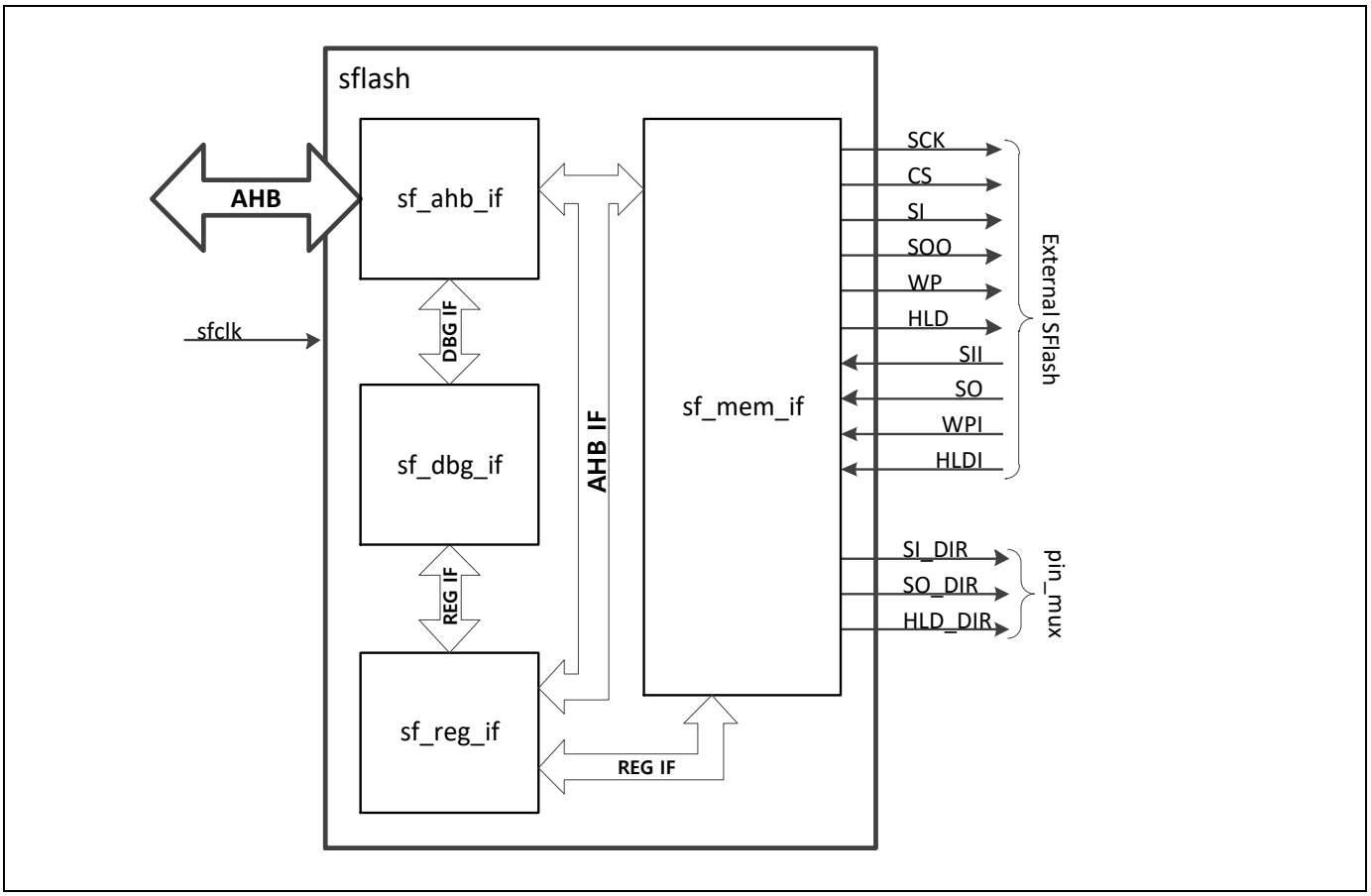


Figure 4-55 Block Diagram of SFI

4.2.15.1 PIN Description

Table 4-9 describes the interrupt assignments.

Table 4-9 Interrupt Assignments

Name	I/O	Description
sfclk	I	SFI clock
SF_SEL	I	SFI memory area selection (0x60000000 ~ 0x6FFFFFFF)
REG_SEL	I	SFI register area selection (0x70000000 ~ 0x70000FFF)
SCK	O	SFI clock
CS	O	SFI chip selection
SI	O	SFI serial data output 0
SOO	O	SFI serial data output 1
WP	O	SFI serial data output 2
HLD	O	SFI serial data output 3
SII	I	SFI serial data input 0
SOO	I	SFI serial data input 1
WPI	I	SFI serial data input 2
HLDI	I	SFI serial data input 3
SI_DIR	O	SI pad direction control (0: Output/ 1: Input)
SO_DIR	O	SO pad direction control (0: Output/ 1: Input)
HLD_DIR	O	HLD/WP pad direction control (0: Output/ 1: Input)

4.2.15.2 Functional Description

SFI supports single and quad mode. In single mode, SI is always output and SO is input. In quad mode, SI, SO, WP, and HLD are bi-directional in quad mode and FSM controls the direction.

You need to check RDSR[0](busy) = 0 before executing the command because there is no FIFO in SFI module.

Also, you can set pad BMODE = 1 to boot with an external serial flash.

4.2.15.2.1 Single Mode

4.2.15.2.1.1 Read Operation

Figure 4-56 illustrates the read operation of single mode.

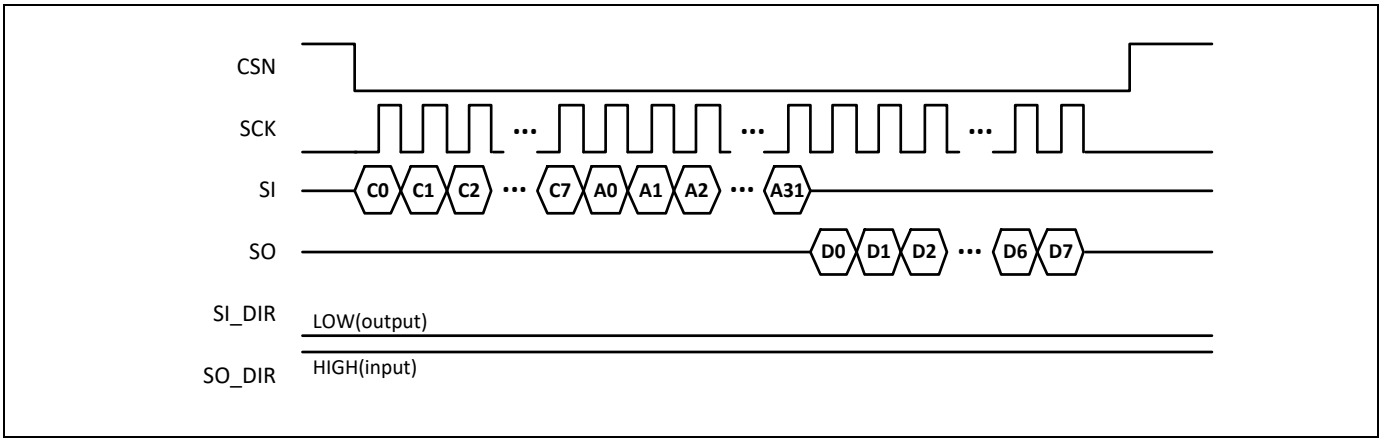


Figure 4-56 Read Operation of Single Mode

4.2.15.2.1.2 Write Operation

Figure 4-57 illustrates the write operation of single mode.

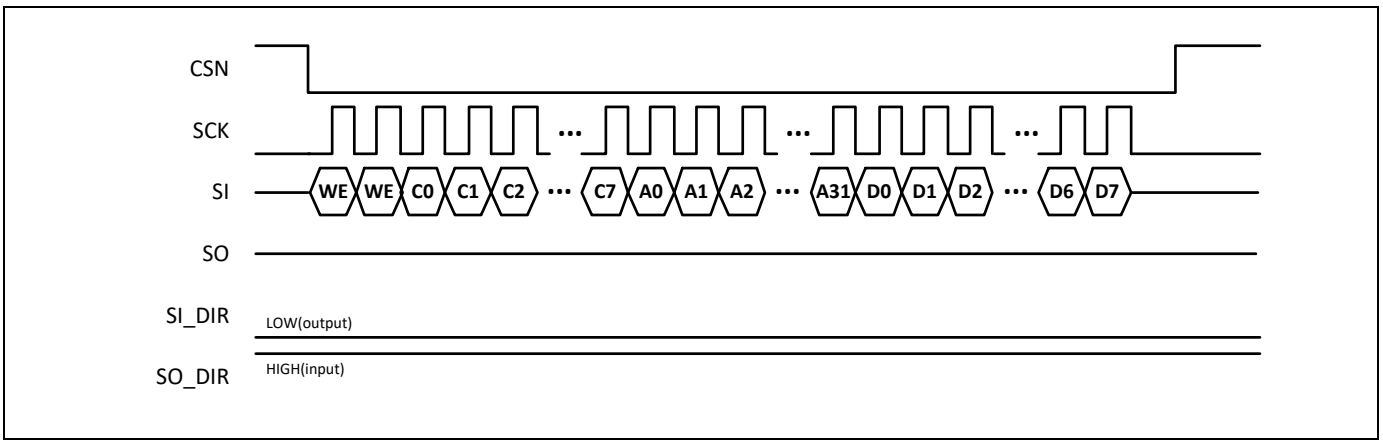


Figure 4-57 Write Operation of Single Mode

4.2.15.2.2 Quad Mode

4.2.15.2.2.1 Read Operation

Figure 4-58 illustrates the read operation of quad mode.

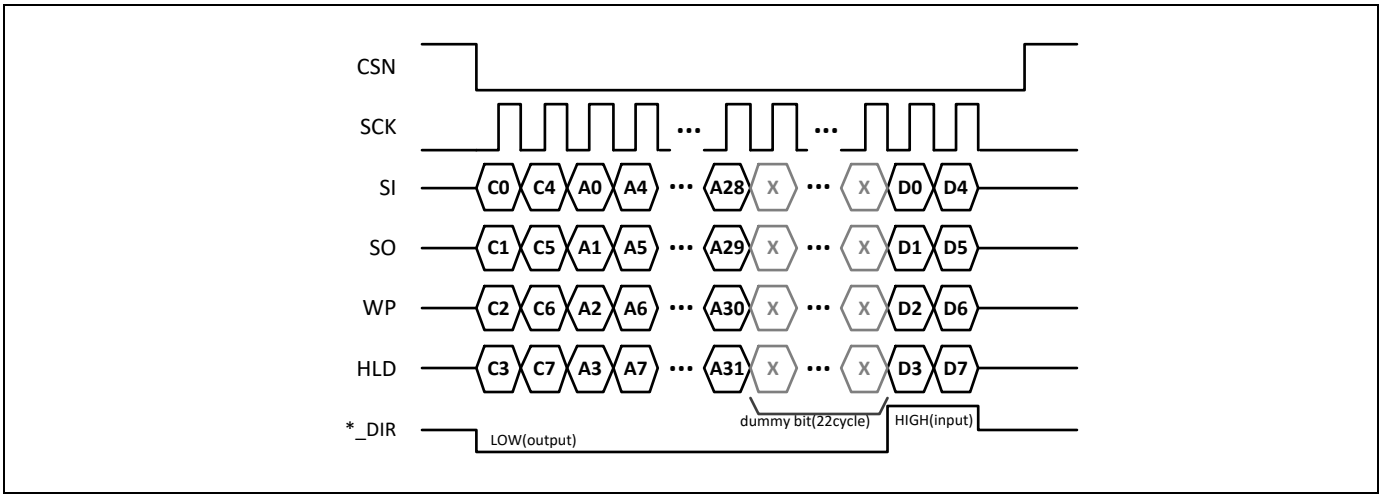


Figure 4-58 Read Operation of Quad Mode

4.2.15.2.2.2 Write Operation

Figure 4-59 illustrates the write operation of quad mode.

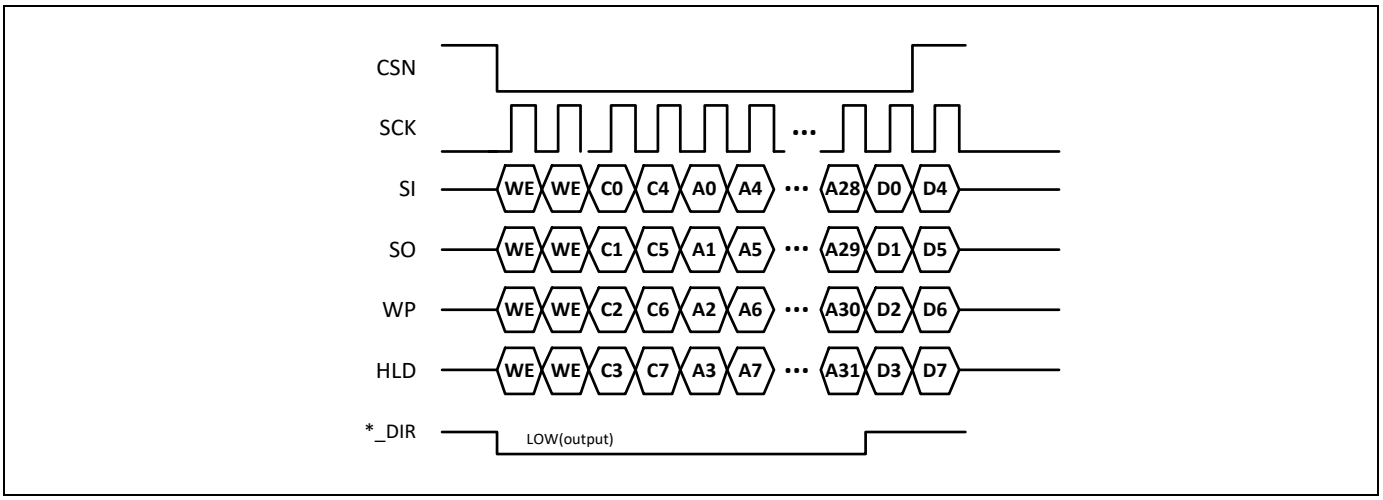


Figure 4-59 Write Operation of Quad Mode

4.2.15.3 Register Description

This section describes the register map information and its associated registers.

4.2.15.3.1 Register Map Summary

- Base Address: 0x7000_0000

Register	Offset	Description	Reset Value
SFCON0	0x0004	Serial Flash Control Register	0x0008_060A
ERASE_ADDRESS	0x0010	Erase Address	0xFFFF_FFFF
PROT_ADDRESS	0x0014	Protection Address	0x3800_0000
CMD0	0x001C	Command0	0xD820_D860
CMD1	0x0020	Command1	0x0001_0505
CMD2	0x0024	Command2	0x029F_0604
CMD3	0x0028	Command3	0x0B0B_FF03
CMD4	0x002C	Command4	0xFFFF_FFFF
CMD5	0x007C	Command5	0x0000_3639
Sector_Erase	0x005E	Sector Erase (64 KB)	0x0000_0000
MODE	0x0074	Mode Change	0x0000_0000
RDID	0x00AC	Read Vendor ID	0x0000_0000
Block_Erase	0x00BE	Block Erase (4 KB)	0x0000_0000
Chip_Erase	0x00CE	Chip Erase	0x0000_0000
RDSR	0x00DC	Read Status Register	0x0000_0000
WRDI	0x00DD	Write Disable	0x0000_0000
WREN	0x00EE	Write Enable	0x0000_0000
PROT_DIS	0x00F0	Unprotect	0x0000_0000
PROT_EN	0x00F1	Protect	0x0000_0000

NOTE: If reserved or empty addresses in the register map are changed, S1SBP6A cannot guarantee normal operation.

4.2.15.3.1.1 SFCON0

- Base Address: 0x7000_0000
- Address = Base Address + 0x0004, Reset Value = 0x0008_060A

Name	Bit	Type	Description	Reset Value
WP_reg	[31]	RW	Write protect 0: Write protect 1: Write unprotect	0x0
async_enb	[29]	RW	Always 0	0x0
atmel_en	[19]	RW	Atmel command use (always 1)	0x1
page_en	[15]	RW	Page programming enable 0: Byte programming 1: Page programming	0x0
PAGE	[11:8]	RW	Page Unit 000: 4 bytes 1 page 001: 8 bytes 1 page 010: 16 bytes 1 page 011: 32 bytes 1 page 100: 64 bytes 1 page 101: 128 bytes 1 page 110: 256 bytes 1 page 111: No support	0x6
HS	[7]	RW	Half clock shift (always 0)	0x0
single_hsrd	[5]	RW	High-speed single read (High speed read : ~33 MHz)	0x0
er_wait	[4]	RW	Erase Wait 0: Do not wait to complete the erase operation after erase command (Do not busy check) 1: Wait to complete the erase operation after erase command (busy check)	0x0
Pre_charge	[3:0]	RW	Pre charging time control Pre charge time = (pre_charge[3:0]+1) * (1/sfclk)	0xA

4.2.15.3.1.2 ERASE_ADDRESS

- Base Address: 0x7000_0000
- Address = Base Address + 0x0010, Reset Value = 0xFFFF_FFFF

Name	Bit	Type	Description	Reset Value
Erase_address	[31:0]	RW	Erase address	0xFFFF_FFFF

4.2.15.3.1.3 PROT_ADDRESS

- Base Address: 0x7000_0000
- Address = Base Address + 0x0014, Reset Value = 0xFFFF_FFFF

Name	Bit	Type	Description	Reset Value
PROT_address	[31:0]	RW	Protection address	0xFFFF_FFFF

4.2.15.3.1.4 Registered Command Registers

4.2.15.3.1.4.1 CMD0

- Base Address: 0x7000_0000
- Address = Base Address + 0x001C, Reset Value = 0x3800_0000

Name	Bit	Type	Description	Reset Value
reg_4pio	[31:24]	RW	Quad mode setting command	0x38
RSVD0	[23:0]	RW	Reserved	0x000000

4.2.15.3.1.4.2 CMD1

- Base Address: 0x7000_0000
- Address = Base Address + 0x0020, Reset Value = 0xD820_D860

Name	Bit	Type	Description	Reset Value
RSVD0	[31:24]	RW	Reserved	0xD8
reg_be	[23:16]	RW	Block (4 KB) erase command	0x20
reg_se	[15:8]	RW	Sector (64 KB) erase command	0xD8
reg_ce	[7:0]	RW	Chip erase command	0x60

4.2.15.3.1.4.3 CMD2

- Base Address: 0x7000_0000
- Address = Base Address + 0x0024, Reset Value = 0x0x0001_0505

Name	Bit	Type	Description	Reset Value
Reserved0	[31:8]	RW	Reserved	0x000105
reg_rdsr	[7:0]	RW	Read status register command	0x05

4.2.15.3.1.4.4 CMD3

- Base Address: 0x7000_0000
- Address = Base Address + 0x0028, Reset Value = 0x029F_0604

Name	Bit	Type	Description	Reset Value
reg_pg	[31:24]	RW	Page program command	0x02
reg_rdid	[23:16]	RW	Vendor ID read command	0x9F
reg_wren	[15:8]	RW	Write enable command	0x06
reg_wrdi	[7:0]	RW	Write disable command	0x04

4.2.15.3.1.4.5 CMD4

- Base Address: 0x7000_0000
- Address = Base Address + 0x002C, Reset Value = 0x0B0B_FF03

Name	Bit	Type	Description	Reset Value
reg_read4p	[31:24]	RW	Quad mode read command	0x0B
reg_hsread	[23:16]	RW	High-speed single mode read command	0x0B
reg_fr	[15:8]	RW	single mode setting	0xFF
reg_read	[7:0]	RW	Single mode read command	0x03

4.2.15.3.1.4.6 CMD5

- Base Address: 0x7000_0000
- Address = Base Address + 0x007C, Reset Value = 0x0000_3639
- Unit: 1 sector (64 KB) (PROT_ADDRESS)

Name	Bit	Type	Description	Reset Value
RSVD0	[31:16]	RW	Reserved	0x0000
reg_prot	[15:8]	RW	Protect command	0x36
reg_unprot	[7:0]	RW	Unprotect command	0x39

4.2.15.3.1.5 Flash Command Registers

4.2.15.3.1.5.1 Sector_Erase

- Base Address: 0x7000_0000
- Address = Base Address + 0x005E, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
Sector_Erase	[7:0]	W	Sector erase	0x0000_0000

4.2.15.3.1.5.2 MODE

- Base Address: 0x7000_0000
- Address = Base Address + 0x0074, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD0	[3]	W	Reserved	0x0000_0000
Quad_mode	[2]	W	Quad_mode	0x0000_0000
RSVD1	[1]	W	Reserved	0x0000_0000
Single_mode	[0]	W	Single_mode (SFCON0[5]=0: Normal, 1: High-speed single)	0x0000_0000

4.2.15.3.1.5.3 RDID (Only Single Mode)

- Base Address: 0x7000_0000
- Address = Base Address + 0x00AC, Reset Value = 0x0100_a743

Name	Bit	Type	Description	Reset Value
Vendor_ID	[31:0]	R	Read vendor ID	0x0100_a743

4.2.15.3.1.5.4 Block_Erase

- Base Address: 0x7000_0000
- Address = Base Address + 0x00BE, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
Block_Erase	[7:0]	W	Block erase	0x0000_0000

4.2.15.3.1.5.5 Chip_Erase

- Base Address: 0x7000_0000
- Address = Base Address + 0x00CE, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
Chip_Erase	[7:0]	W	Chip erase	0x0000_0000

4.2.15.3.1.5.6 RDSR (Only Single Mode)

- Base Address: 0x7000_0000
- Address = Base Address + 0x00DC, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RDSR	[7:0]	R	Read status register	0x0000_0000

4.2.15.3.1.5.7 WRDI

- Base Address: 0x7000_0000
- Address = Base Address + 0x00DD, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
WRDI	[7:0]	W	Write disable	0x0000_0000

4.2.15.3.1.5.8 WREN

- Base Address: 0x7000_0000
- Address = Base Address + 0x00EE, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
WREN	[7:0]	W	Write enable	0x0000_0000

4.2.15.3.1.5.9 PROT_DIS

- Base Address: 0x7000_0000
- Address = Base Address + 0x00F0, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
PROT_DIS	[7:0]	W	Protection disable	0x0000_0000

4.2.15.3.1.5.10 PROT_EN

- Base Address: 0x7000_0000
- Address = Base Address + 0x00F1, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
PROT_EN	[7:0]	W	Protection enable	0x0000_0000

4.2.16 Interrupts

S1SBP6A contains 119 Interrupt Request (IRQ) lines, one Non-Maskable Interrupt (NMI), and one event signal. *Table 4-10* describes the interrupt assignments. Cortex-M4 processors have an RXEV input signal. If software uses the Wait for Event (WFE) instruction to put the processor to sleep, then the received event at RXEV wakes up the processor. The RXEV is connected to DMA-done signal of the μDMAC. This enables the processor to wake up from WFE sleep when the DMA process completes.

Table 4-10 Interrupt Assignments

IRQ/NMI	Device	IRQ/NMI	Device	IRQ/NMI	Device	IRQ/NMI	Device
NMI	Watchdog	29	RTC2	59	DMA CH23	89	GPIO12
0	BOR	30	FPU	60	DMA CH24	90	GPIO13
1	UART0	31	SRP0	61	DMA CH25	91	GPIO14
2	UART1	32	SRP1	62	DMA CH26	92	GPIO15
3	UART2	33	Delay Monitor	63	DMA CH27	93	GPIO16
4	SPI0	34	AES	64	DMA CH28	94	GPIO17
5	SPI1	35	External Wakeup	65	DMA CH29	95	GPIO18
6	SPI2	36	DMA CH0	66	DMA CH30	96	GPIO19
7	SPI3	37	DMA CH1	67	DMA CH31	97	GPIO1A
8	SPI4	38	DMA CH2	68	GPIO0 Combined	98	GPIO1B
9	I2C0	39	DMA CH3	69	GPIO1 Combined	99	GPIO1C
10	I2C1	40	DMA CH4	70	GPIO2 Combined	100	GPIO1D
11	I2C2	41	DMA CH5	71	GPIO00	101	GPIO1E
12	I2C3	42	DMA CH6	72	GPIO01	102	GPIO1F
13	I2C4	43	DMA CH7	73	GPIO02	103	GPIO20
14	Timer0	44	DMA CH8	74	GPIO03	104	GPIO21
15	Timer1	45	DMA CH9	75	GPIO04	105	GPIO22
16	Timer2	46	DMA CH10	76	GPIO05	106	GPIO23
17	Timer3	47	DMA CH11	77	GPIO06	107	GPIO24
18	Timer4	48	DMA CH12	78	GPIO07	108	GPIO25
19	Timer5	49	DMA CH13	79	GPIO08	109	GPIO26
20	Timer6	50	DMA CH14	80	GPIO09	110	GPIO27
21	PWM Timer0	51	DMA CH15	81	GPIO0A	111	GPIO28
22	Dual Timer	52	DMA CH16	82	GPIO0B	112	GPIO29
23	AFE Controller	53	DMA CH17	83	GPIO0C	113	GPIO2A

IRQ/NMI	Device	IRQ/NMI	Device	IRQ/NMI	Device	IRQ/NMI	Device
24	SRC	54	DMA CH18	84	GPIO0D	114	GPIO2B
25	DMA Error	55	DMA CH19	85	GPIO0E	115	GPIO2C
26	Embedded Flash	56	DMA CH20	86	GPIO0F	116	GPIO2D
27	RTC0	57	DMA CH21	87	GPIO10	117	GPIO2E
28	RTC1	58	DMA CH22	88	GPIO11	118	GPIO2F

4.2.17 Phase-Locked Loop

Phase-Locked Loop (PLL) in S1SBP6A is a clock generation IP which synthesizes wide range frequency output. It consists of Phase-Frequency Detector (PFD), charge pump, Voltage-Controlled Oscillator (VCO), 6-bit pre-divider, 7-bit main-divider, 2-bit scaler, and Automatic Frequency Control (AFC).

Use the following equations to determine the relationship between the output frequency (F_{FOUT}) and input frequency (F_{FIN}).

$$F_{FVCO} = \frac{m \times F_{FIN}}{p}$$

$$F_{FOUT} = \frac{m \times F_{FIN}}{p \times 2^s}, 1 \le p \le 63, 16 \le m \le 127, 0 \le s \le 3$$

Where, p, m, and s are the divider values for pre-divider, main-divider, and scaler respectively.

4.2.17.1 Register Description

This section describes the register map information and its associated registers.

4.2.17.1.1 Register Map Summary

- Base Address: 0x4001_C000

Register	Offset	Description	Reset Value
PLL_CTRL0	0x0600	PLL_CTRL0	0x0001_8804
PLL_CTRL1	0x0604	PLL_CTRL1	0x001E_8641
PLL_STATUS	0x0608	PLL_STATUS	0x0000_0000

NOTE: If reserved or empty addresses in the register map are changed, S1SBP6A cannot guarantee normal operation.

4.2.17.1.1.1 PLL_CTRL0

- Base Address: 0x4001_C000
- Address = Base Address + 0x0600, Reset Value = 0x0001_8804

Name	Bit	Type	Description	Reset Value
TEST_DIV	[16:15]	RW	FOUT test output divider value for test mode 00: No divide 01: Divided by 2 10: Divided by 4 11: Divided by 8	0x0000_0003
TEST_EN	[14]	RW	PLL test mode control 0: Test mode disable 1: Test mode enable	0x0000_0000
LOCK_CON_REV	[13:12]	RW	Reserved for Lock Detector	0x0000_0000
LRD_EN	[11]	RW	LDR control 0: LDR disable 1: LDR enable	0x0000_0001
PBIAS_CTRL	[10]	RW	PBIAS pull-down initial voltage control 0: 0.50*VDD 1: 0.67*VDD	0x0000_0000
PBIAS_CTRLEN	[9]	RW	PBIAS voltage pull-down control 0: Pull-down disable 1: Pull-down enable	0x0000_0000
VCO_BOOST	[8]	RW	VCO boost control 0: VCO boost enable 1: VCO boost disable	0x0000_0000
FOUT_MASK	[7]	RW	Scaler's re-initialization time control 0: Bypass FOUT 1: Mask FOUT	0x0000_0000
AFC_INITSEL	[6]	RW	AFC initial delay select 0: Nominal delay 1: Increased delay	0x0000_0000
FSEL	[5]	RW	FEEDOUT signal select 0: Monitor FREF through FEEDOUT 1: Monitor FEED through FEEDOUT	0x0000_0000
FEED_EN	[4]	RW	FEEDOUT signal monitoring control 0: Monitoring enable 1: Monitoring disable	0x0000_0000
AFC_ENB	[3]	RW	PLL Automatic Frequency Calibration (AFC) control 0: AFC is enabled and VCO is automatically calibrated. 1: AFC is disabled and VCO is manually calibrated by EXTAFC.	0x0000_0000
LOCK_EN	[2]	RW	PLL Lock Detector control	0x0000_0001

Name	Bit	Type	Description	Reset Value
			0: Lock Detector disable 1: Lock Detector enable	
BYPASS	[1]	RW	PLL bypass control. 0: PLL normal operation mode. 1: PLL bypass mode	0x0000_0000
RSVD0	[0]	R	Reserved	0x0000_0000

4.2.17.1.1.2 PLL_CTRL1

- Base Address: 0x4001_C000
- Address = Base Address + 0x0604, Reset Value = 0x001E_8641

Name	Bit	Type	Description	Reset Value
PLL_RESERVE_SIGNAL	[31:28]	RW	PLL reserved.	0x0000_0000
EXTAFC	[27:23]	RW	External AFC control	0x0000_0000
LOCK_CON_DLY	[22:21]	RW	Lock detector setting of detection resolution	0x0000_0000
LOCK_CON_OUT	[20:19]	RW	Lock detector setting of output margin	0x0000_0003
LOCK_CON_IN	[18:17]	RW	Lock detector setting of input margin	0x0000_0003
ICP	[16:15]	RW	Charge-pump current control	0x0000_0001
PLL_S	[14:13]	RW	PLL scaler control	0x0000_0000
PLL_M	[12:6]	RW	PLL main-divider control	0x0000_0019
PLL_P	[5:0]	RW	PLL pre-divider control	0x0000_0001

4.2.17.1.1.3 PLL_STATUS

- Base Address: 0x4001_C000
- Address = Base Address + 0x0608, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
AFC_CODE	[5:1]	R	AFC output code monitor	0x0000_0000
LOCK	[0]	R	PLL lock monitor	0x0000_0000

4.2.18 High Speed Oscillator

High Speed Oscillator (HSOSC) in S1SBP6A is a clock generation IP which is an RC oscillator with output frequency of 24.576 MHz. It can be trimmed during fabrication and can optionally calibrate with an external 32.768 kHz clock to generate the precise clock frequency. HSOSC consists of oscillator core, current reference, and Frequency-Locked Loop (FLL).

4.2.18.1 Register Description

This section describes the register map information and its associated registers.

4.2.18.1.1 Register Map Summary

- Base Address: 0x4001_C000

Register	Offset	Description	Reset Value
HSOSC_CTRL	0x060C	HSOSC_CTRL	0x0000_0A00

NOTE: If reserved or empty addresses in the register map are changed, S1SBP6A cannot guarantee normal operation.

4.2.18.1.1.1 HSOSC_CTRL

- Base Address: 0x4001_C000
- Address = Base Address + 0x060C, Reset Value = 0x0000_0A00

Name	Bit	Type	Description	Reset Value
TOL	[11:10]	RW	Frequency tolerance of internal Frequency-Locked Loop	0x0000_0002
CAL	[9:2]	RW	Frequency control bits	0x0000_0080
MODE	[1]	RW	HSOSC operation mode control. 0: Frequency control by CAL 1: Frequency calibration by internal real-time Frequency-Locked Loop	0x0000_0000
RSVD0	[0]	R	Reserved	0x0000_0000

4.2.19 Low Speed Oscillator

Low Speed Oscillator (HSOSC) in S1SBP6A is a clock generation IP which is an RC oscillator with output frequency of 4.096 MHz. It can be trimmed during fabrication and can generate precise clock frequency by calibration with external 32.768 kHz clock optionally. LSOSC consists of oscillator core, current reference, and Frequency-Locked Loop (FLL).

4.2.19.1 Register Description

This section describes the register map information and its associated registers.

4.2.19.1.1 Register Map Summary

- Base Address: 0x4001_C000

Register	Offset	Description	Reset Value
LSOSC_CTRL	0x0610	LSOSC_CTRL	0x0000_0A00

NOTE: If reserved or empty addresses in the register map are changed, S1SBP6A cannot guarantee normal operation.

4.2.19.1.1.1 LSOSC_CTRL

- Base Address: 0x4001_C000
- Address = Base Address + 0x0610, Reset Value = 0x0000_0A00

Name	Bit	Type	Description	Reset Value
TOL	[11:10]	RW	Frequency tolerance of internal Frequency-Locked Loop	0x0000_0002
CAL	[9:2]	RW	Frequency control bits	0x0000_0080
MODE	[1]	RW	HSOSC operation mode control 0: Frequency control by CAL 1: Frequency calibration by internal real-time Frequency-Locked Loop	0x0000_0000
RSVD0	[0]	R	Reserved	0x0000_0000

4.3 System Control

4.3.1 Startup Sequence

Figure 4-60 illustrates the startup sequence of S1SBP6A.

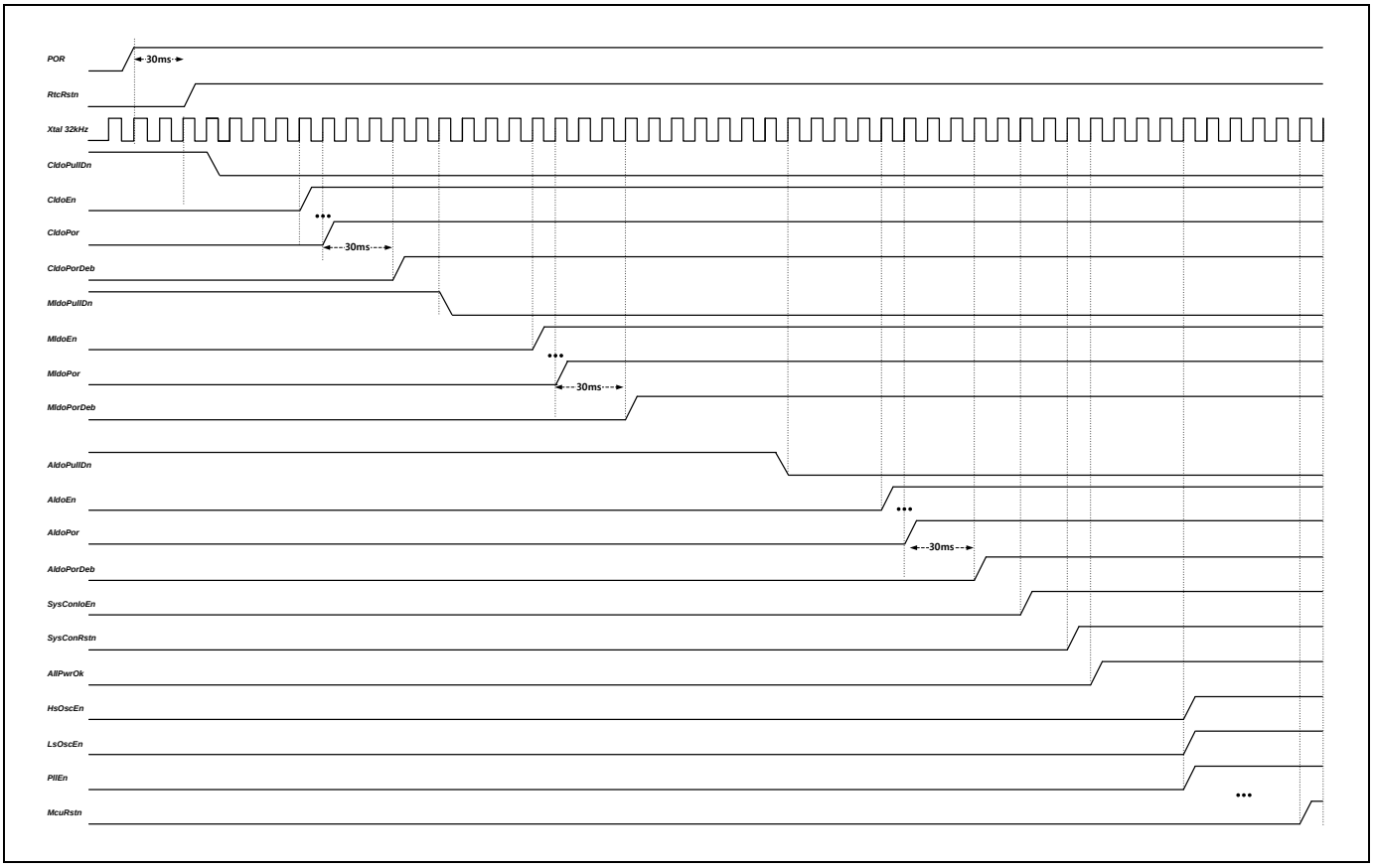


Figure 4-60 Startup Sequence of RTC Logic

The sequence begins when external 3 V powers, AVDD33, and DVDD33 are supplied. Power-on Reset (POR) that is used as the reset of RTC logic is released after AVDD33 is settled down and it is de-bounced in 30 ms using 32.768 kHz clock from external crystal input. The de-bounced POR initiates the power sequencer of RTC logic. Internal LDOs, CLDO, MLDO, PLDO, and ALDO are turned on sequentially. Each LDO outputs LDO POR indicating the readiness of LDO power supply. Those LDO PORs are also de-bounced in 30 ms for stable power supply operation. After releasing of the last POR from ALDO, IO power switches, which supply powers of normal GPIOs and isolated crystal IO, are turned on. Finally, reset toward system controller is released. System controller logic starts after releasing the reset from RTC logic. The reset from RTC logic is de-bounced in 30 ms and then internal oscillators such as LSOSC and HSOSC are turned on. MCU reset is released after ticking by number of several clocks.

4.3.2 Power-On Reset (POR) and Brown-Out Reset (BOR)

BOR and POR have simple hysteresis architectures which have a high-level reference and a low-level reference. BOR detects a brown-out voltage when power supply is falling down and sends BOR state signal to RTC logic. In the same way, POR detects a power-on voltage when power supply is rising up and sends POR state signal to RTC logic.

As illustrated in *Figure 4-61* , BOR has upper threshold and lower threshold. If external power is 3 V with ± 10 % variation, the upper threshold of BOR is 2.7 V (2.6 V + 0.1 V) and the lower threshold is 2.6 V. The upper threshold of POR is 1.62 V and the lower threshold is 1.52 V (1.62 V –0.1 V).

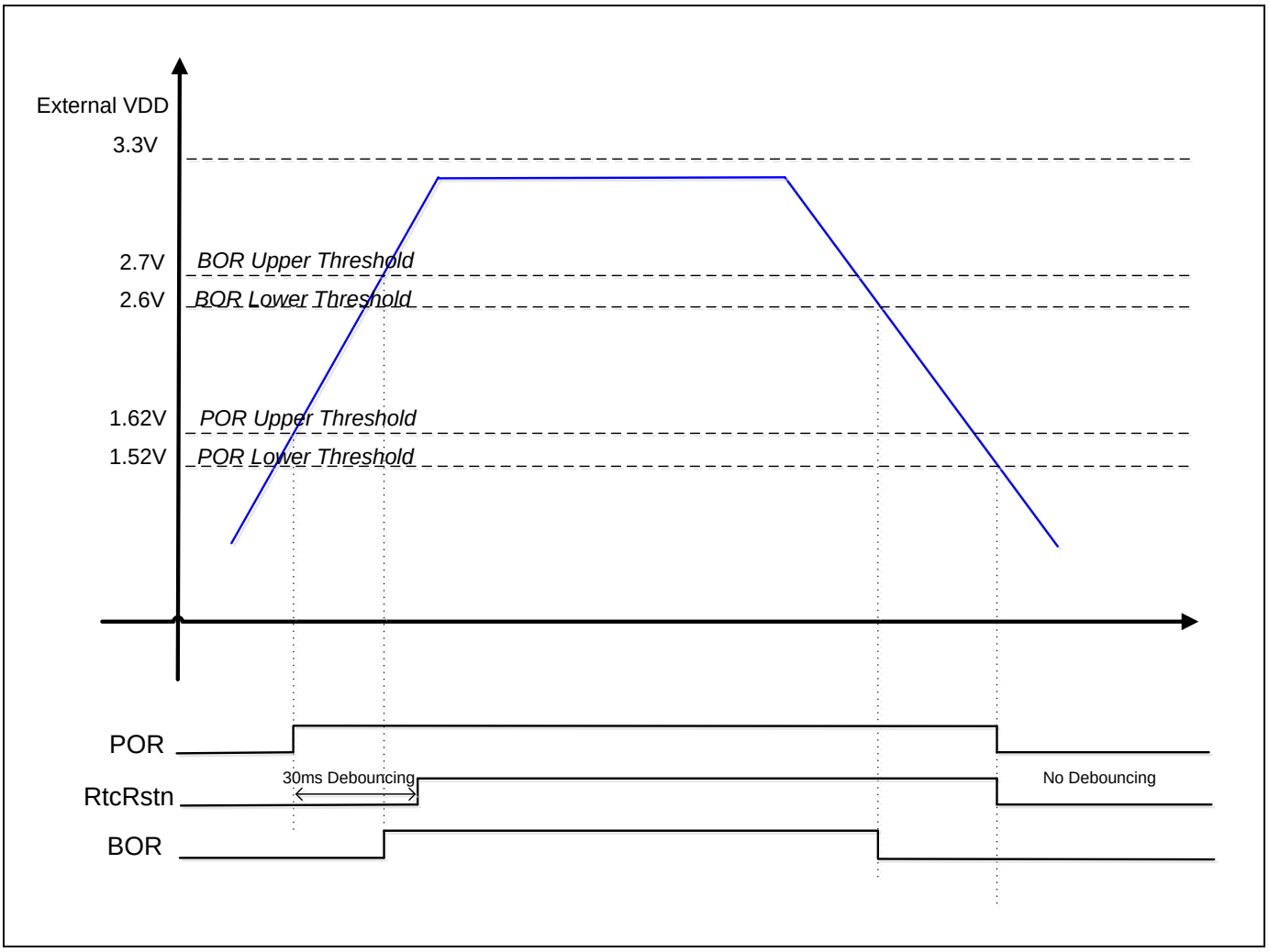


Figure 4-61 BOR and POR Threshold Levels and Reset Signals

4.3.3 Clock Management Unit

S1SBP6A includes Clock Management Unit (CMU) which manages clock gating controls to reduce the active current consumption.

CMU supports the following four features:

- Source clock selectivity for MCU, peripherals, and AFE controller
- Clock divider programmability of MCU, peripheral, and SAR-ADC sampling clock
- Clock gating capability of separated clock domains
- Clock selectivity of serial interfaces

Figure 4-62 illustrates the clock tree of S1SBP6A.

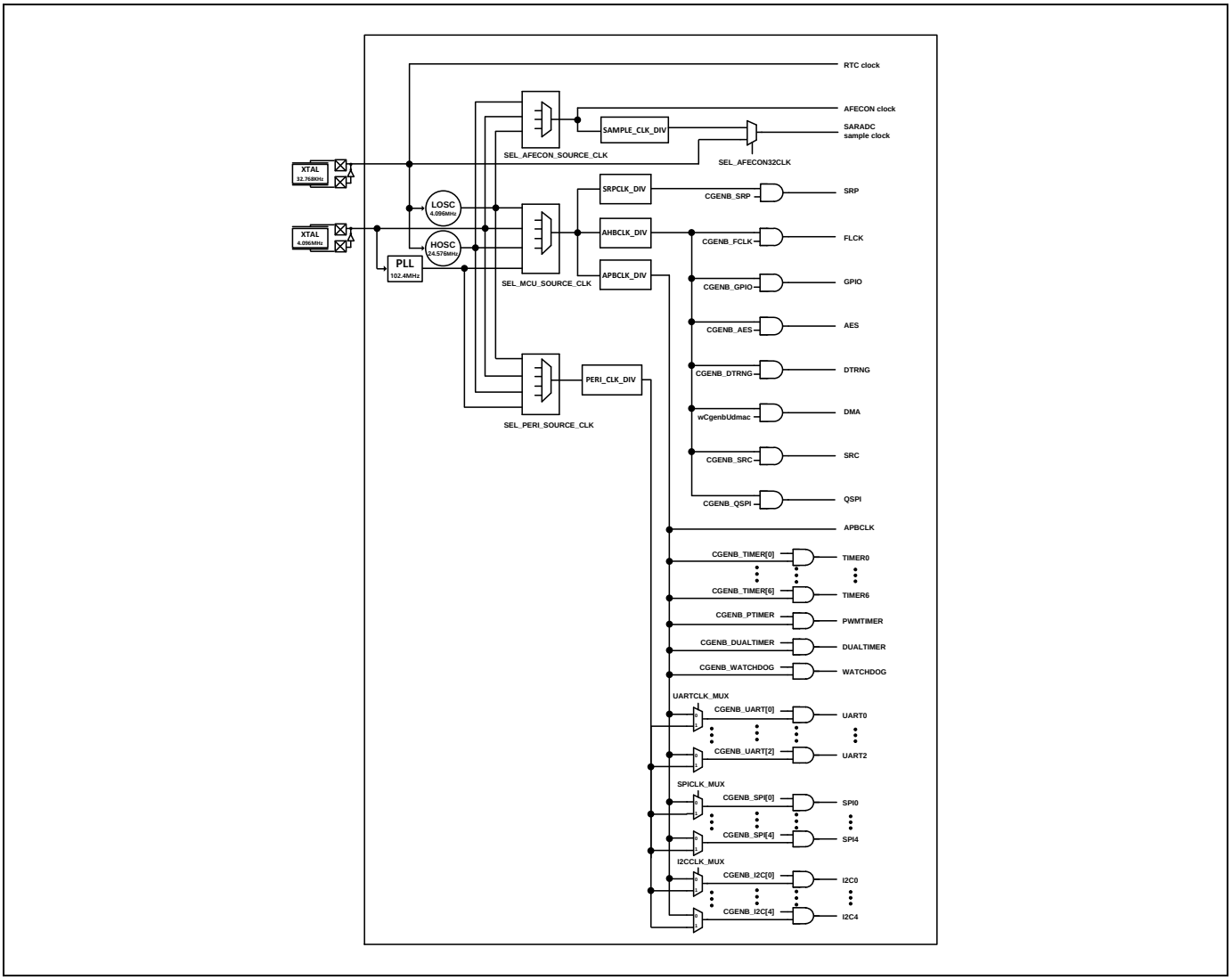


Figure 4-62 Clock Tree of S1SBP6A

4.3.3.1 Register Description

This section describes the register map information and its associated registers.

4.3.3.1.1 Register Map Summary

- Base Address: 0x4001_C000

Register	Offset	Description	Reset Value
MCU_CLK_CTRL	0x0100	MCU Clock Control	0x0020_2022
MCU_CLK_GATE	0x0104	MCU Clock Gate Control	0x000B_FFFF
PERI_CLK_CTRL	0x0110	PERI Clock Control	0x0000_0022
PERI_CLK_GATE	0x0114	PERI Clock Gate Control	0x0000_1FFF
PERI_CLK_MUX	0x0118	PERI Clock Mux	0x0000_0000
AFE_CLK_CTRL	0x0120	AFE Clock Control	0x0000_3006
WAIT_PERI_CLK_GATE	0x0918	WAIT_PERI Clock Gate Control	0x0

NOTE: If reserved or empty addresses in the register map are changed, S1SBP6A cannot guarantee normal operation.

4.3.3.1.1.1 MCU_CLK_CTRL

- Base Address: 0x4001_C000
- Address = Base Address + 0x0100, Reset Value = 0x0020_2022

Name	Bit	Type	Description	Reset Value
RSVD0	[31:28]	RW	Reserved	0x0000_0000
SRPCLK_DIV	[27:20]	RW	SRP clock divide value can be selected from 2 to 254. If you select 0 or 1, then the clock is divided by 1.	0x0000_0002
APBCLK_DIV	[19:12]	RW	APB clock divide value can be selected from 2 to 254. If select 0 or 1 then clock is divided by 1.	0x0000_0002
AHBCLK_DIV	[11:4]	RW	AHB clock divide value can be selected from 2 to 254. If select 0 or 1 then clock is divided by 1.	0x0000_0002
RSVD1	[3:2]	RW	Reserved	0x0000_0000
SEL_MCU_SOURCE_CLK	[1:0]	RW	*Source clock selection 3: PLL clock 2: HS OSC clock 1: External 4.096MHz xtal clock 0: LS OSC clock	0x0000_0002

NOTE: AHBCLK_DIV, APBCLK_DIV and SRPCLK_DIV should be same.

4.3.3.1.1.2 MCU_CLK_GATE

- Base Address: 0x4001_C000
- Address = Base Address + 0x0104, Reset Value = 0x000B_FFFF

Name	Bit	Type	Description	Reset Value
RSVD0	[23:20]	RW	Reserved	0x0000_0000
CG_BYPASS	[19]	RW	* Clock gate bypass (active high) 1: Clock enabled even though CGENB is activated. (FCLK, SRP, GPIO, UDMAC, DTRNG, AES, SRC, and QSPI) 0: Clock gated by CGENB	0x0000_0001
UDMAC_ACG_EN	[18]	RW	* UDMAC auto clock gate enable (active high) 1: Auto clock gate 0: Manual clock gate	0x0000_0000
CGENB_WATCHDOG	[17]	RW	* Watchdog clock gate (active low) 1: Clock enabled 0: Clock gated	0x0000_0001
CGENB_DUALTIMER	[16]	RW	* Dual timer clock gate (active low) 1: Clock enabled 0: Clock gated	0x0000_0001
CGENB_PTIMER	[15:14]	RW	* PWM timer clock gate (active low) 1: Clock enabled 0: Clock gated	0x0000_0003
CGENB_TIMER	[13:8]	RW	* Timer clock gate (active low) 1: Clock enabled 0: Clock gated	0x0000_003F
CGENB_QSPI	[7]	RW	* QSPI clock gate (active low) 1: Clock enabled 0: Clock gated	0x0000_0001
CGENB_SRC	[6]	RW	* SRC clock gate (active low) 1: Clock enabled 0: Clock gated	0x0000_0001
CGENB_AES	[5]	RW	* AES clock gate (active low) 1: Clock enabled 0: Clock gated	0x0000_0001
CGENB_DTRNG	[4]	RW	* DTRNG clock gate (active low) 1: Clock enabled 0: Clock gated	0x0000_0001
CGENB_UDMAC	[3]	RW	* UDMAC manual clock gate (active low) 1: Clock enabled 0: Clock gated	0x0000_0001
CGENB_GPIO	[2]	RW	* GPIO clock gate (active low) 1: Clock enabled	0x0000_0001

Name	Bit	Type	Description	Reset Value
			0: Clock gated	
CGENB_SRP	[1]	RW	* SRP clock gate (active low) 1: Clock enabled 0: Clock gated	0x0000_0001
CGENB_FCLK	[0]	RW	* Free running clock gate (active low) 1: Clock enabled 0: Clock gated	0x0000_0001

4.3.3.1.1.3 PERI_CLK_CTRL

- Base Address: 0x4001_C000
- Address = Base Address + 0x0110, Reset Value = 0x0000_0022

Name	Bit	Type	Description	Reset Value
RSVD0	[15:12]	RW	Reserved	0x0000_0000
PERI_CLK_DIV	[11:4]	RW	Peripheral clock divide value can be selected from 2 to 254. If select 0 or 1 then clock is divided by 1.	0x0000_0002
RSVD1	[3:2]	RW	Reserved	0x0000_0000
SEL_PERI_SOURCE_CLK	[1:0]	RW	*Source clock selection 3: PLL clock 2: HS OSC clock 1: External 4.096 MHz xtal clock 0: LS OSC clock	0x0000_0002

4.3.3.1.1.4 PERI_CLK_GATE

- Base Address: 0x4001_C000
- Address = Base Address + 0x0114, Reset Value = 0x0000_1FFF

Name	Bit	Type	Description	Reset Value
RSVD0	[15:13]	RW	Reserved	0x0000_0000
CGENB_I2C	[12:8]	RW	* I2C clock gate (active low) 1: Clock enabled 0: Clock gated	0x0000_001F
CGENB_SPI	[7:3]	RW	* SPI clock gate (active low) 1: Clock enabled 0: Clock gated	0x0000_001F
CGENB_UART	[2:0]	RW	* UART clock gate (active low) 1: Clock enabled 0: Clock gated	0x0000_0007

4.3.3.1.1.5 PERI_CLK_MUX

- Base Address: 0x4001_C000
- Address = Base Address + 0x0118, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD0	[15:13]	RW	Reserved	0x0000_0000
I2CCLK_MUX	[12:8]	RW	*[8]: I2C0 control [9]: I2C1 control [10]: I2C2 control [11]: I2C3 control [12]: SPI4 control 0: Select MCU clock 1: Select Peri clock NOTE: I2C source clock is same as MCU source clock.	0x0000_0000
SPICLK_MUX	[7:3]	RW	*[3]: SPI0 control [4]: SPI1 control [5]: SPI2 control [6]: SPI3 control [7]: SPI4 control 0: Select MCU clock 1: Select Peri clock	0x0000_0000
UARTCLK_MUX	[2:0]	RW	*[0]: UART0 control [1]: UART1 control [2]: UART2 control 0: Select MCU clock 1: Select Peri clock	0x0000_0000

4.3.3.1.1.6 AFE_CLK_CTRL

- Base Address: 0x4001_C000
- Address = Base Address + 0x0120, Reset Value = 0x0000_3006

Name	Bit	Type	Description	Reset Value
RSVD0	[23:20]	RW	Reserved	0x0000_0000
SAMPLE_CLK_DIV	[19:4]	RW	AFECON clock divide value can be selected from 2 to 65534. If select 0 or 1 then clock is divided by 1.	0x0000_0300
SEL_AFECON32CLK	[3]	RW	*Sample clock selection 0: Select internal generated clock that is divided by SAMPLE_CLK_DIV with AFECON_SOURCE_CLK 1: Select external 32.768 kHz xtal clock	0x0000_0000
AFECON_DIV_ON	[2]	RW	*AFECON Divider 0: Internal counter for divider is off 1: Internal counter for divider is on	0x0000_0001
SEL_AFECON_SOURCE_CLK	[1:0]	RW	*Source clock selection 3: Reserved 2: HS OSC clock 1: External 4.096 MHz xtal clock 0: LS OSC clock	0x0000_0002

4.3.3.1.1.7 WAIT_PERI_CLK_GATE

- Base Address: 0x4001_C000
- Address = Base Address + 0x0918, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
WAIT_PERI_CGEN	[0]	RW	* Wait_Peri clock gate (active high) 1: Clock gated 0: Clock enabled	0x0000_0000

4.3.4 Power Management Unit

S1SBP6A includes Power Management Unit (PMU) which manages the modes of system operation. PMU executes the power on-off controls of sub-blocks and mode change control to reduce power consumption.

S1SBP6A has 22 power domains including one always-on domain and 21 power-gating or power-off domains. RTC block is always-on to perform real-time clocking function and managing startup sequence of the chip. The rest of the chip except RTC block is turned off in LPM0, the lowest power mode of S1SBP6A described in *Table 4-11* by shutting down the internal LDOs. MCU has 12 power domains including MCU system, Cortex-M4 core, Flash and Cache, and eight 32 KB SRAMs. Cortex-M4 core is retained under the low-power modes except LPM4. In these four low-power modes, all information is saved for the processor to continue the program which is stopped before power down. Power gating is not applied and only clocks are gated in LPM4. For the memories, Flash Cache and MCU SRAMs can be power-gated or retained. SRP includes six power domains including one SRP logic, one SRP TCM, and four SRP DMEMs. SRP logic supports only power-gating option and all of SRP SRAMs can be power-gated or retained. *Table 4-11* describes the modes of operation available in S1SBP6A.

Table 4-11 Low-Power Modes of S1SBP6A

Mode Name	Entry	Wakeup Sources	Descriptions
LPM0	LPM2 + PLDOEN_CTRL = 1 + PLDOPULLDN_CTRL = 0 + RTCMODEREADY = 1	BMODE RTC interrupts	RTC on, Others off
LPM1	LPM2 + STANDBYREADY = 1	GPIO00-1F pins Timer0 interrupt Uart0 interrupt SPI0 interrupt I2C0 interrupt	RTC/SYSCON on, Flash sleep, Others off
LPM2	SYSPWR_CTRL = 1 + PMU_CTRL = 1 + SLEEPDEEP =1 + WFI	Timer0 interrupt Uart0 interrupt SPI0 interrupt I2C0 interrupt DMA requests	MCU system retention, Cortex core retention, Flash on
LPM3	PMU_CTRL = 1 + SLEEPDEEP =1 + WFI	Timer0 interrupt Uart0 interrupt SPI0 interrupt I2C0 interrupt General Interrupts	MCU system on, Cortex core retention
LPM4	PMU_CTRL = 1 + WFI	Timer0 interrupt Uart0 interrupt SPI0 interrupt I2C0 interrupt General interrupts	Cortex core clock gating

NOTE: SLEEPDEEP is the [2] bit field of System Control Register (SCR) of Cortex-M4 core. For more information on SLEEPDEEP, refer to Cortex-M4 Devices Generic User Guide, *http://infocenter.arm.com/help/topic/com.arm.doc.dui0553a/DUI0553A_cortex_m4_dgug.pdf*

Following are the modes of operation available in S1SBP6A:

- LPM0 (Low-Power Mode 0)

S1SBP6A supports ultra-low power mode named LPM0. Only RTC block is alive and all other blocks are turned off in this mode. The chip enters LPM0 by setting PLDOEN_CTRL, SYSPWR_CTRL, SLEEPDEEP, and RTCMODEREADY bits into 1 and PLDOPULLDN_CTRL bit into 0 and executing WFI or WFE system function. Processor wakes up by toggling of BMODE or RTC Interrupts.

- LPM1 (Low-Power Mode 1)

S1SBP6A enters into LPM1 by setting SYSPWR_CTRL, SLEEPDEEP, and STANDBYREADY bits into 1, and executing WFI or WFE system function. At the same time, GPIO00 to GPIO1F pins should be low. In LPM1, Only RTC block and system control logic are alive. Flash is in sleep mode. Processor wakes up either for any changes in GPIO00 to GPIO1F pins or when any Wait-Peri interrupts occur.

- LPM2 (Low-Power Mode 2)

S1SBP6A enters into LPM2 by setting SYSPWR_CTRL and SLEEPDEEP bit into 1 and executing WFI or WFE system function. In LPM2, Cortex core and MCU system block goes to retention mode. In this mode, processor wakes up by Wait-Peri interrupts from UART0, I2C0, Timer0, SPI0, and DMA requests.

- LPM3 (Low-Power Mode 3)

S1SBP6A enters into LPM3 by setting SLEEPDEEP bit into 1 and executing WFI or WFE system function. In this mode, Cortex core goes to retention state where all the data of flip-flops are retained. In LPM3, processor wakes up by any interrupts described in *Table 4-10* or by wake up events.

- LPM4 (Low-Power Mode 4)

S1SBP6A enters into LPM4 by WFI or WFE system function. Core clock is gated in LPM4 and processor wakes up when any interrupts described in *Table 4-10* or by wake up events.

4.3.4.1 Register Description

This section describes the register map information and its associated registers.

4.3.4.1.1 Register Map Summary

- Base Address: 0x4001_9000 (KA)

Register	Offset	Description	Reset Value
PMU_KA_DLY_CTRL0	0x0000	KA_PWR_SEQUENCE_DELAY_CTRL 0	0x11
PMU_KA_DLY_CTRL1	0x0004	KA_PWR_SEQUENCE_DELAY_CTRL 1	0x11
PMU_KA_LDO_CTRL	0x0008	KA_LDO_CTRL	0xF0
PMU_KA_LDO_POR_STATUS	0x000C	KA_LDO_POR_STATUS	0x00
PMU_KA_MANUAL_CTRL	0x0010	KA_MANUAL_CTRL	0x00
PMU_KA_32K_XTAL_CON	0x00F0	KA_32K_XTAL_CON	0x1
PMU_IOPWR_CTRL	0x00F4	KA_IOPWR_CTRL	0x1

NOTE: If reserved or empty addresses in the register map are changed, S1SBP6A cannot guarantee normal operation.

- Base Address: 0x4001_C000 (SYSCON)

Register	Offset	Description	Reset Value
PMU_SYSCON_CTRL	0x0000	SYSCON_CTRL	0x0380
PMU_SYSCON_DLY_CTRL	0x0004	SYSCON_PWR_SEQUENCE_DELAY_CTRL	0x111111
PMU_MCU_DLY_CTRL	0x0008	MCU_PWR_SEQUENCE_DELAY_CTRL	0x0AFF0A0A
PMU_SYSCON_DLY_EN	0x000C	SYSCON_DELAY_ENABLE	0x00C
PMU_SYSCON_FAST_BOOT	0x0014	SYSCON_FAST_BOOT_ENABLE	0x0014
PMU_MCU_PD_CTRL	0x0200	PMU_PD_CTRL	0x0000_0000
PMU_MCU_PD_STATUS	0x0204	PMU_MCU_PD_STATUS	0x5BFFF
PMU_MCU_RET_CTRL	0x0208	PMU_RET_CTRL	0x7000_0000
SYSCON_WAKEUP_CTRL	0x0904	SYSCON_WAKEUP_CTRL	0x0
SYSCON_WAKEUP_STATUS_CLEAR	0x0908	SYSCON_WAKEUP_STATUS_CLEAR	0x0
SYSCON_KA_ACCESS	0x914	SYSCON_KA_ACCESS	0x0

4.3.4.1.1.1 PMU_KA_DLY_CTRL 0

- Base Address: 0x4001_9000 (KA)
- Address = Base Address + 0x0000, Reset Value = 0x0000_0011

Name	Bit	Type	Description	Reset Value
DLY_SYSCONCTRL_PU	[7:4]	RW	* Delay control after IO enable when powering up	0x0000_0000
DLY_SYSCONRSTN_PD	[3:0]	RW	* Delay control after SysCon reset is asserted High	0x0000_0000

4.3.4.1.1.2 PMU_KA_DLY_CTRL 1

- Base Address: 0x4001_9000 (KA)
- Address = Base Address + 0x0004, Reset Value = 0x0000_0011

Name	Bit	Type	Description	Reset Value
DLY_SYSCONCTRL_PD	[7:4]	RW	* Delay control after SysCon reset is asserted Low when powering down	0x0000_0000
DLY_ALDOEN_PD	[3:0]	RW	* Delay control after Aldo enable is Low when powering down	0x0000_0000

4.3.4.1.1.3 PMU_KA_LDO_CTRL

- Base Address: 0x4001_9000 (KA)
- Address = Base Address + 0x0008, Reset Value = 0x0000_00F0

Name	Bit	Type	Description	Reset Value
ALDOPULLDN_CTRL	[7]	RW	ALDO pull-down control	0x0000_0001
PLDOPULLDN_CTRL	[6]	RW	PLDO pull-down control	0x0000_0001
MLDOPULLDN_CTRL	[5]	RW	MLDO pull-down control	0x0000_0001
CLDOPULLDN_CTRL	[4]	RW	CLDO pull-down control	0x0000_0001
ALDOEN_CTRL	[3]	RW	0: ALDO disable 1: ALDO enable	0x0000_0000
PLDOEN_CTRL	[2]	RW	0: PLDO disable 1: PLDO enable	0x0000_0000
MLDOEN_CTRL	[1]	RW	0: MLDO disable 1: MLDO enable	0x0000_0000
CLDOEN_CTRL	[0]	RW	0: CLDO disable 1: CLDO enable	0x0000_0000

4.3.4.1.1.4 PMU_KA_LDO_POR_STATUS

- Base Address: 0x4001_9000 (KA)
- Address = Base Address + 0x000C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ALDO_POR_STATUS	[3]	RW	ALDO POR status 0: ALDO POR down 1: ALDO POR on	0x0000_0000

4.3.4.1.1.5 PMU_KA_MANUAL_CTRL

- Base Address: 0x4001_9000 (KA)
- Address = Base Address + 0x0010, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
MANUAL_LDOPULLDN_CTRL	[6]	RW	Manually PLDO, ALDO pull-down control	0x0000_0000
PBORREF_ONOFF_PRD	[5:4]	RW	The period of automatic turn on and off of POR, BOR, and BGR. 00: 50 ms 01: 100 ms 10: 500 ms 11: 1 s	0x0000_0000
AUTO_PBORREF_ONOFF	[2]	RW	Automatic on-off control for POR, BOR, and BGR. 0: POR, BOR, and BGR are always-on. 1: POR, BOR, and BGR are turned on and off automatically with the period which is defined by PBORREF_ONOFF_PRD.	–
MANUAL_LDO_CTRL	[0]	RW	Manually PLDO, ALDO Enable Control 0: Disable 1: Enable	–

4.3.4.1.1.6 PMU_KA_32K_XTAL_CON

- Base Address: 0x4001_9000 (KA)
- Address = Base Address + 0x00F0, Reset Value = 0x0000_0001

Name	Bit	Type	Description	Reset Value
EN	[0]	RW	32 kHz Xtal Enable	0x0000_0001

4.3.4.1.1.7 PMU_KA_IOPWR_CTRL

- Base Address: 0x4001_9000 (KA)
- Address = Base Address + 0x00F4, Reset Value = 0x0000_0001

Name	Bit	Type	Description	Reset Value
MANUAL_IOEN_CTRL	[1]	RW	GPIO power manual cntrol	0x0000_0000
SYSCON_IOEN	[0]	RW	GPIO power control 0: Disable 1: Enable	0x0000_0001

4.3.4.1.1.8 PMU_SYSCON_CTRL

- Base Address: 0x4001_C000 (SYSCON)
- Address = Base Address + 0x0000, Reset Value = 0x0000_0380

Name	Bit	Type	Description	Reset Value
MANUAL_OSC_CTRL	[10]	RW	* Manual OSC, PLL control 0: Auto control 1: Manual control	0x0000_0000
PLLEN_SEQ	[9]	RW	* PLL control on SysCon powering up sequence 0: PLL Disable 1: PLL Enable	0x0000_0001
LOSCEN_SEQ	[8]	RW	* Low speed oscillator control on SysCon Powering up sequence 0: LOSC Disable 1: LOSC Enable	0x0000_0001
HOSCEN_SEQ	[7]	RW	* High speed oscillator control on SysCon Powering up sequence 0: HOSC Disable 1: HOSC Enable	0x0000_0001
PLLEN_CTRL	[6]	RW	* PLL control on SysCon powering down sequence 0: PLL Disable 1: PLL Enable	0x0000_0000
LOSCEN_CTRL	[5]	RW	* Low speed oscillator control on SysCon Powering down sequence 0: LOSC Disable 1: LOSC Enable	0x0000_0000
HOSCEN_CTRL	[4]	RW	* High speed oscillator control on SysCon powering down sequence 0: HOSC Disable 1: HOSC Enable	0x0000_0000
STANDBYREADY	[1]	RW	* Enter standby mode 0: Disable 1: Enable	0x0000_0000
RTCMODEREADY	[0]	RW	* Enter RTC mode 0: Disable 1: Enable	0x0000_0000

4.3.4.1.1.9 PMU_SYSCON_DLY_CTRL

- Base Address: 0x4001_C000 (SYSCON)
- Address = Base Address + 0x0004, Reset Value = 0x0000_1111

Name	Bit	Type	Description	Reset Value
DLY_PRSTNISON_PD	[15:12]	RW	* Delay control for Flash power down on SysCon powering down sequence.	0x0000_0001
DLY_PRSTNISON_PU	[11:8]	RW	* Delay control for Flash power down on SysCon powering up sequence.	0x0000_0001
DLY_MCURSTN_PU	[7:4]	RW	* Delay control for MCU reset released on SysCon powering up sequence.	0x0000_0001
DLY_CLKCON_PU	[3:0]	RW	* Delay control for oscillator, PLL enable control on SysCon powering up sequence.	0x0000_0001

4.3.4.1.1.10 PMU_MCU_DLY_CTRL

- Base Address: 0x4001_C000 (SYSCON)
- Address = Base Address + 0x0008, Reset Value = 0x0AFF_0A0A

Name	Bit	Type	Description	Reset Value
DLY_RSTN	[31:24]	RW	* Delay reset state when powering up or down	0x0000_000A
DLY_PD	[23:16]	RW	* Delay control for super cutoff power gating	0x0000_00FF
DLY_RET	[15:8]	RW	* Delay retention state when powering up or down	0x0000_000A
DLY_ISO	[7:0]	RW	* Delay isolation state when powering up or down	0x0000_000A

4.3.4.1.1.11 PMU_SYSCON_DLY_EN

- Base Address: 0x4001_C000 (SYSCON)
- Address = Base Address + 0x000C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
PMU_SYSCON_DLY_EN	[0]	RW1C	* PMU_SYSCON_DLY_CTRL enable 0: Disable 1: Enable	0x0000_0000

4.3.4.1.1.12 PMU_SYSCON_PD_CTRL

- Base Address: 0x4001_C000 (SYSCON)
- Address = Base Address + 0x0200, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CHG_PWR_STATE	[19]	RW	* Change Power State - Toggling this register starts power sequence of PMU with PMU_SYSCON_PD_CTRL and PMU_SYSCON_RET_CTRL registers. Power control is updated by changing this bit after writing power down and retention registers (PMU_SYSCON_PD_CTRL and PMU_SYSCON_RET_CTRL).	0x0000_0000
PD_FLASH	[17]	RW	Power down control for Flash when entering LPM1 0: Power on 1: Power down	–
PD_DECIM	[16]	RW	* Power down control for memory inside decimation filter 0: Power on 1: Power down	0x0000_0000
PD_FCACHE	[15]	RW	* Power down control for memory inside Flash memory controller 0: Power on 1: Power down	0x0000_0000
PD_DSP	[13]	RW	* Power down control for SRP logic 0: Power on 1: Power down	0x0000_0000
PD_DSP_DMEM	[12:9]	RW	* Power down control for SRP data memory banks (4 banks) 0: Power on 1: Power down	0x0000_0000
PD_DSP_TMEM	[8]	RW	* Power down control for SRP tight coupled 0: Power on 1: Power down	0x0000_0000
PD_MCU_SRAM	[7:0]	RW	* Power down control for MCU memory banks (8 banks) 0: Power on 1: Power down	0x0000_0000

4.3.4.1.1.13 PMU_SYSCON_PD_STATUS

- Base Address: 0x4001_C000 (SYSCON)
- Address = Base Address + 0x0204, Reset Value = 0x0005_BFFF

Name	Bit	Type	Description	Reset Value
PD_DECIM_STATUS	[16]	RO	* Status of memory inside decimation filter 0: Off 1: On	0x0000_0001
PD_FCACHE_STATUS	[15]	RO	* Status of memory inside Flash memory controller 0: Off 1: On	0x0000_0001
PD_DSP_STATUS	[13]	RO	* Status of PD_DSP 0: Off 1: On	0x0000_0001
PD_DSP_DMEM_STATUS	[12:9]	RO	* Status of SRP data memory 0: Off 1: On	0x0000_000F
PD_DSP_TMEM_STATUS	[8]	RO	* Status of SRP tightly coupled memory 0: Off 1: On	0x0000_0001
PD_MCU_SRAM_STATUS	[7:0]	RO	* Status of MCU memory 0: Off 1: On	0x0000_00FF

4.3.4.1.1.14 PMU_SYSTEM _RET_CTRL

- Base Address: 0x4001_C000 (SYSCON)
- Address = Base Address + 0x0208, Reset Value = 0x7000_0000

Name	Bit	Type	Description	Reset Value
DSP_RESETn_REG	[21]	RW	* SRP reset control register	0x0000_0001
SYSPWR_CTRL_EN	[19]	RW	* Power retention control for MCU system power domain 0: MCU system power domain always on 1: MCU system power domain enters into retention mode (according to PMU FSM)	0x0000_0000
RET_DECIM	[16]	RW	* Retention mode control for memory inside decimation filter 0: Normal operation mode 1: Retention mode	0x0000_0000
RET_FCACHE	[15]	RW	* Retention mode control for cache memory inside Flash memory controller 0: Normal operation mode 1: Retention mode	0x0000_0000
RET_DSP_DMEM	[12:9]	RW	* Power retention control for SRP data memory banks (4 banks) 0: Normal operation mode 1: Retention mode	0x0000_0000
RET_DSP_TMEM	[8]	RW	* Power retention control for SRP tightly coupled memory banks (1 banks) 0: Normal operation mode 1: Retention mode	0x0000_0000
RET_MCU_SRAM	[7:0]	RW	* Power retention control for MCU data memory banks (8 banks) 0: Normal operation mode 1: Retention mode	0x0000_0000

4.3.4.1.1.15 SYSCON_WAKEUP_CTRL

- Base Address: 0x4001_C000 (SYSCON)
- Address = Base Address + 0x0904, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
SYSCON_WAKEUP_STATUS	[31:0]	RO	* GPIO wake up status in LPM1	0x0000_0000

4.3.4.1.1.16 SYSCON_WAKEUP_STATUS_CLEAR

- Base Address: 0x4001_C000 (SYSCON)
- Address = Base Address + 0x0908, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
SYSCON_WAKEUP_STATUS_CLEAR	[0]	RW	* GPIO wake up status clear	0x0000_0000

4.3.4.1.1.17 SYSCON_KA_ACCESS

- Base Address: 0x4001_C000 (SYSCON)
- Address = Base Address + 0x0914, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
KA_ACCESS	[0]	RW	* KA Domain APB bus access control 0: Enable 1: Disable	0x0000_0000

5 Analog Front End

This chapter includes the following sections:

- Overview
- Functional description

5.1 Overview

Figure 5-1 illustrates the block diagram of Analog Front End (AFE).

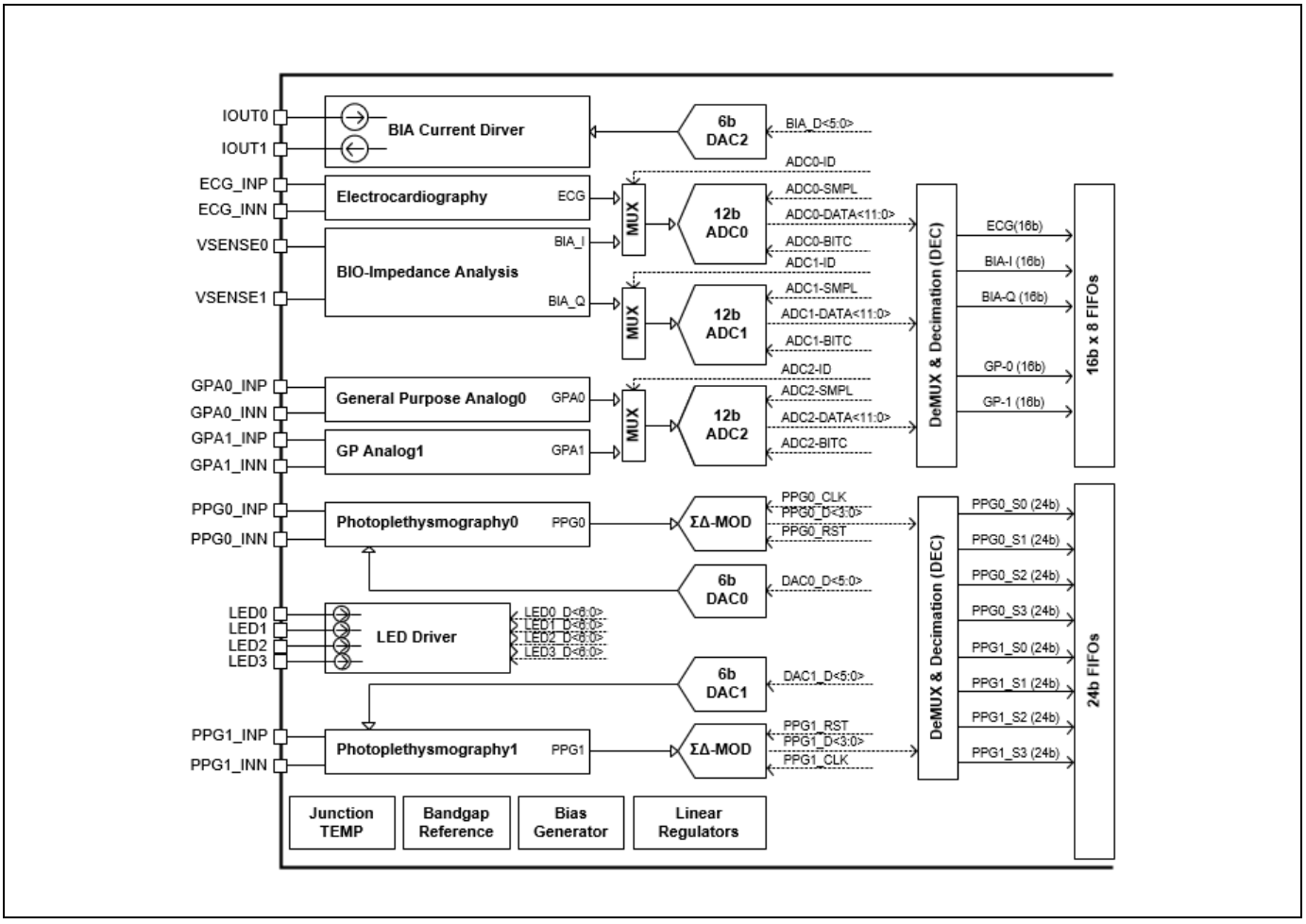


Figure 5-1 Block Diagram of Analog Front End

S1SBP6A integrates multiple low-power AFEs to support wide range of bio-sensor applications. It includes an ECG readout, a BIA readout, a GSR readout, and two PPG readouts along with four LED drivers. In addition, several analog interfaces are provided for general usage. These includes a time multiplexed 12-bit ADC with supporting voltage and current inputs. *Figure 5-1* illustrates the simplified top-level architecture of AFEs in S1SBP6A. The complete AFEs receive power either from a built-in regulator (ALDO) or from an external regulator (through the pins of AVDD33, AVDD33A, and AVDD33_LED). Necessary bias signals for AFEs are generated from a fine-tuned bandgap reference. Output data streams from different AFEs are synchronized with each other and it allows implementing accurate and reliable parameter calculations in digital domain.

Following are the main functional blocks and their description:

- The ECG readout measures bio-potential signals originated from heart. It supports high impedance dry electrodes. Moreover, a built-in HPF at inputs suppresses potential DC offset from electrodes in practice. The complete AFE is optimized for low-noise and low-power consumption. A built-in driver provides bias to the body through electrode.
- The AFE for PPG supports Photo Diode (PD) readout. Along with LED driver, the PD and the AFE measure the reflected or transmitted lights modulated by heartbeat. The AFE operates in a synchronous manner with the LED pulse. It separates up to four different signals per sample before digitization. These four signals from single PD are responses of different wavelengths of LEDs and ambient light. With the help of digital signal processing, real-time ambient light cancellation for PPG is possible which is essential for the applications of heart rate monitoring and SpO2 evaluation. Both PPG readout and LED driver provide wide range of programmability such as LED driving currents, pulse rate and pulse duty, readout gain, and input DC photocurrent cancellation capability. These flexibilities offer wide options for user to trade-off between power consumption and signal quality.
- The AFE for BIA predicts body impedance from measurement of voltage level in different body locations. An (externally) AC-coupled current source with programmable current-levels and frequency is utilized to inject current signals into the body through a pair of current electrodes. The fat inside the body impedes the injected AC current flow. By using another pair of (voltage) electrodes, the BIA AFE readouts voltage signal built across bio-impedance. For body composition analysis, the frequency of current signal can be adjusted from 1 kHz to 1 MHz with fine-grade resolution. The voltage signal received by BIA AFE can be demodulated either in rectified mode (envelope detection) or in I/Q mode (quadrature detection) according to the user preference.
- S1SBP6A includes several General Purpose (GP) analog interfaces to additionally support wide range sensor applications such as measuring temperature, pressure, weight, or light intensity. The GP analog interfaces in S1BP6A contain a 12-bit, up to 8 kSPS ADC cooperating with a highly programmable AFE (GP Analog0) that supports either voltage or current inputs, and a direct external inputs (integrated anti-alias filter, GP Analog1 multiplexing with GP Analog0).
- S1SBP6A also integrates digital control logic to cooperate with AFEs. The function of AFE control logic includes AFE channel separation from ADC outputs, decimation, and data buffering with either 16-bit or 24-bit data format with 16 depths.

- S1SBP6A integrates three identical 12-bit ADCs. Depending on the states of ADCx_ID, each ADC converts two analog signals from AFEs in time multiplexed manner. ADC sample rate is determined by clock signal of ADCx_SMPL and the rate can be 2 kHz as illustrated in *Figure 5-2* for normal sampling mode with a duty cycle = 6.25 % or 16 kHz as illustrated in *Figure 5-3* for oversampling mode with a duty cycle = 50 %.

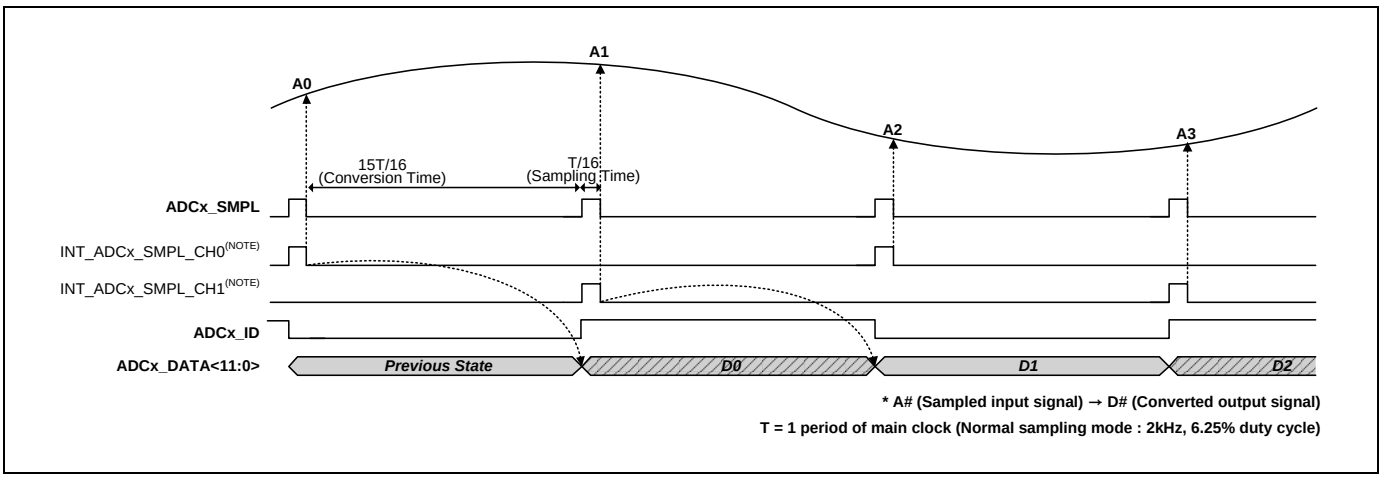


Figure 5-2 Timing Diagram of 12-bit ADC Operating in Normal Sampling Mode

NOTE: Each ADC uses the internal sampling clocks.

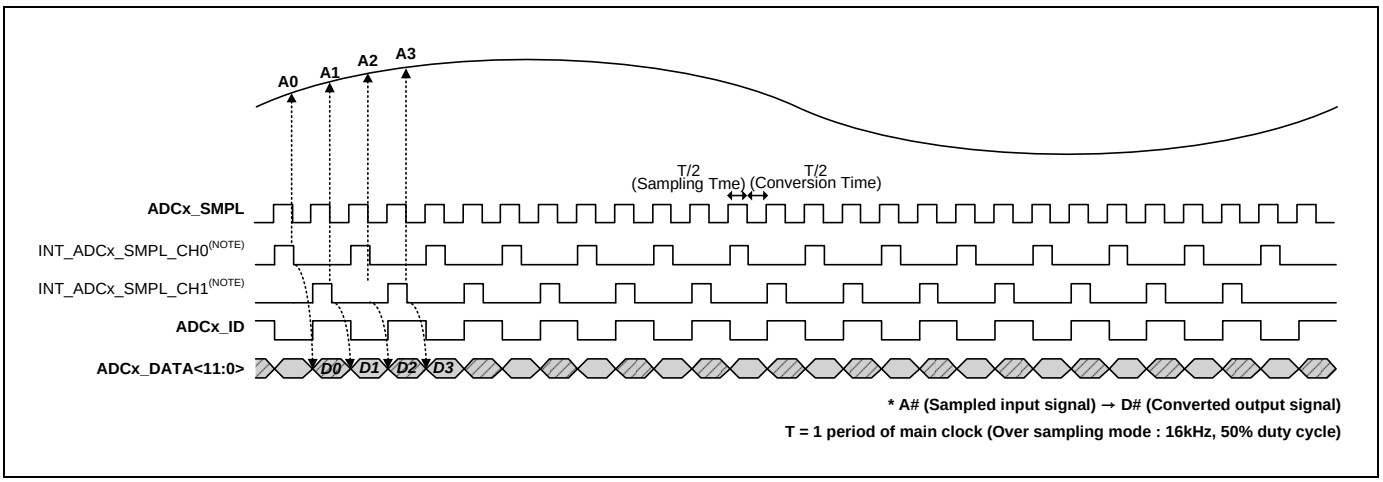


Figure 5-3 Timing Diagram of 12-bit ADC Operating in Oversampling Mode

NOTE: Each ADC uses the internal sampling clocks.

5.2 Functional Description

5.2.1 ECG Readout

5.2.1.1 Overview

ECG readout channel is a low-power integrated AFE dedicated for bio-potential signal acquisition. The supply voltage of ECG readout is 1.1 V and it is regulated by the built-in ALDO. The ECG readout channel illustrated in *Figure 5-4* consists of the following components:

- Input switch matrix that supports the following functions
  - ECG signal acquisition with bipolar electrode montage
  - DC offset measurement of ECG readout chain
  - Built-in square wave signal generation for the readout channel gain measurement.
- A built-in input High-Pass Filter (HPF) to avoid electrode DC offset amplification. This HPF can be bypassed to allow external HPF application. An integrated pair of 20 MΩ resistors provides an option for external HPF with only series capacitors.
- A fully differential chopper-modulated Instrumentation Amplifier (IA) with max. 10 mV_{p-p} input signal swing.
- A Programmable Gain Amplifier (PGA) stage to provide additional signal amplification of from 0 dB to 15.6 dB. This stage also embeds a passive second-order Low Pass Filter (LPF) with –3 dB bandwidth from 75 –250 Hz, to suppress chopping spike signals from IA stage as well as to provide first-order anti-alias filter function for noise suppression.
- A channel buffer with optional (needs two external capacitors, each of 0.1 μF) HPF with –3 dB bandwidth of 0.2 Hz. The register value of ECG_HPF2_EN enables this feature.
- A 12 bit ADC for ECG signal digitization. This ADC can be operated at a rate of either 1 kSPS or 8 kSPS along with digital decimation to provide improved Effective Number of Bits (ENOB).
- A built-in 3 bit DAC with output driver to bias human body through electrode. The output voltage can be varied from 330 –715 mV. The maximum output current drivability of body bias is 10 μA.
- *Figure 5-4* illustrates the block diagram of ECG readout channel.

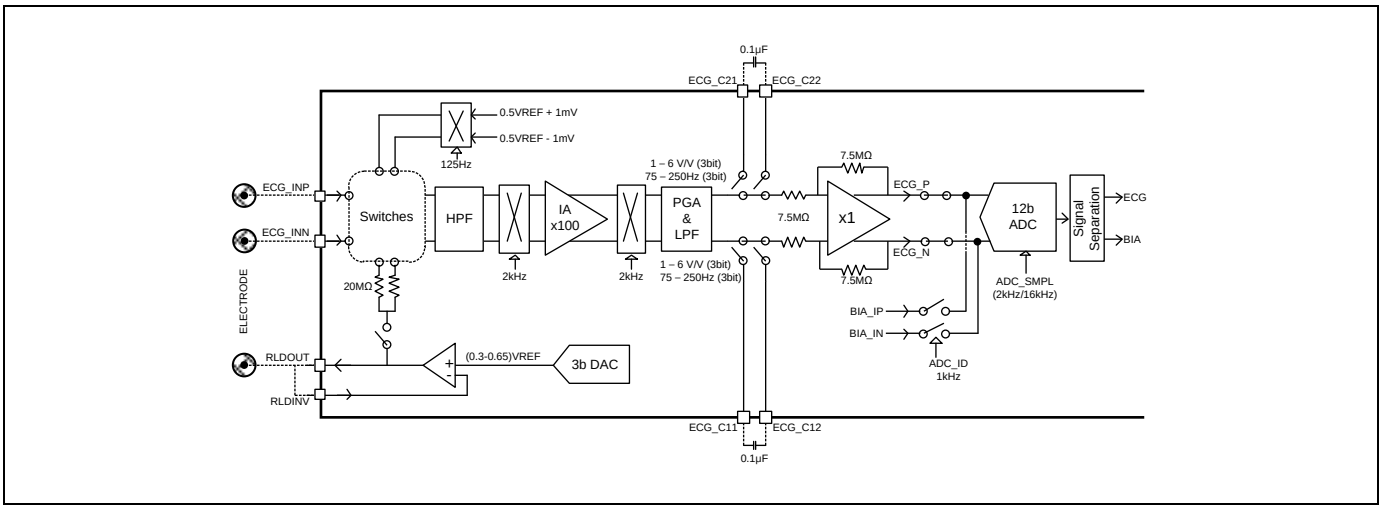


Figure 5-4 Block Diagram of ECG Readout Channel

5.2.1.2 ADC Timing Diagram

ADC0 samples ECG and BIA output signals and converts them into 12 bit data stream (ADC_DATA in *Figure 5-5*). Sampling frequency of ADC can be configured to either 2 kHz or 16 kHz. To differentiate ECG and BIA signals, ADC_ID0 separates the sampled data at the output. When the ADC outputs the signal at a rate of 16 kSPS, a digital decimation is applied to the ADCx_DATA to form 16 bit data format. *Figure 5-5* illustrates the ADC timing diagram for ECG readout channel.

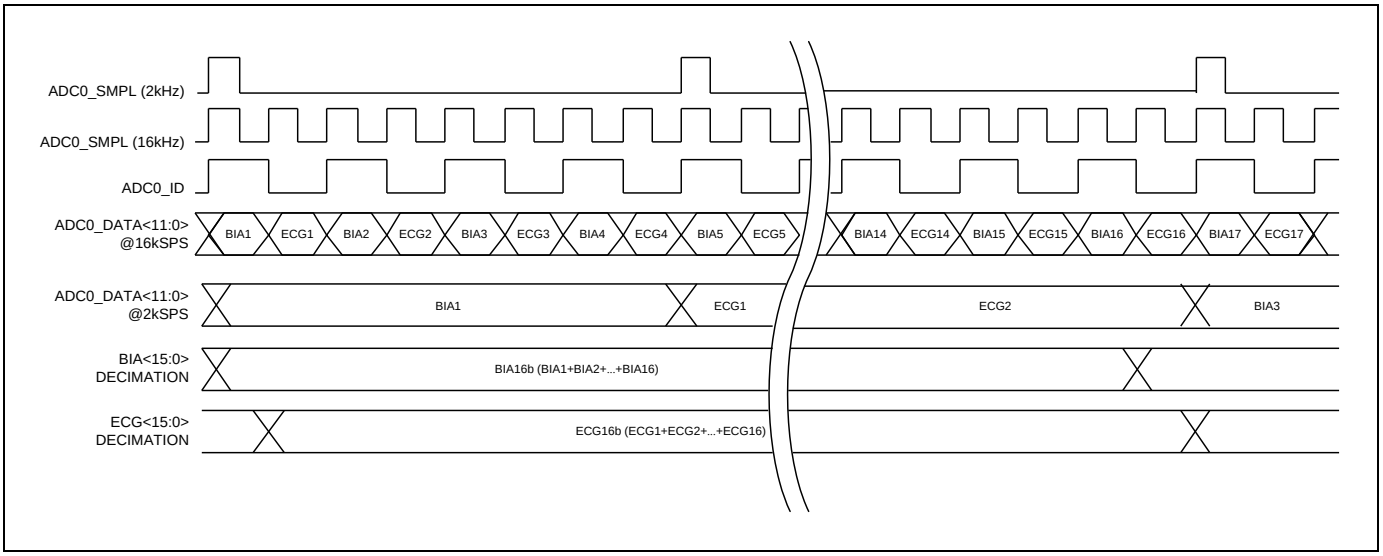


Figure 5-5 ADC Timing Diagram for ECG Readout Channel

5.2.1.3 Register Description

This section describes the register map information and its associated registers.

5.2.1.3.1 Register Map Summary

- Base Address: 0x4001_A100

Register	Offset	Description	Reset Value
ECG_EN	0x0	ECG channel enable control	0x0000_0000
ECG_GAIN	0x4	ECG PGA gain control	0x0000_0000
ECG_BW	0x8	ECG Low-pass filter bandwidth control	0x0000_0000
ECG_SET	0xc	ECG oversampling control register	0x0000_0000
ECG_INIT	0x10	ECG 1st high pass filter initialize to VCM voltage	0x0000_0000
ECG_HPF	0x14	ECG High-pass filter control register	0x0000_0000
ECG_CONT	0x18	ECG test purpose registers	0x0000_0084

NOTE: If reserved or empty addresses in the register map are changed, S1SBP6A cannot guarantee normal operation.

5.2.1.3.1.1 ECG_EN

- Base Address: 0x4001_A100
- Address = default_BASE + 0x0, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ECG_EN	[0]	RW	ECG channel power on/off. 0: power off 1: power on	0x0000_0000

5.2.1.3.1.2 ECG_GAIN

- Base Address: 0x4001_A100
- Address = default_BASE + 0x4, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ECG_GAIN1	[2:0]	RW	ECG channel PGA Gain: 000: x1 001: x1.2 010:x1.6 011: x2 100: x3 101: x4 110: x5 111: x6	0x0000_0000

5.2.1.3.1.3 ECG_BW

- Base Address: 0x4001_A100
- Address = default_BASE + 0x8, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
BW_ECG1	[2:0]	RW	ECG channel LPF BW. 000:250Hz 001:225Hz 010:200Hz 011:180Hz 100:150Hz 101:125Hz 110:100Hz 111:75Hz	0x0000_0000

5.2.1.3.1.4 ECG_SET

- Base Address: 0x4001_A100
- Address = default_BASE + 0xc, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
EN_OVRSMP	[3]	RW	ECG differential output buffer bandwidth control. 1: limit BW 0: Unllimit	0x0000_0000

5.2.1.3.1.5 ECG_INIT

- Base Address: 0x4001_A100
- Address = default_BASE + 0x10, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
INIT	[0]	RW	ECG SC-HPF initiallization 1: short to VCM 0: disable	0x0000_0000

5.2.1.3.1.6 ECG_HPF

- Base Address: 0x4001_A100
- Address = default_BASE + 0x14, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
HPF2_EN	[2]	RW	2nd HPF(Between PGA and Buffer) enable control signal. 1: on, 0: off	0x0000_0001
EXT_HPF_EN	[1]	RW	External HPF connection. 1: Use external Cap + internal 20Mohm 0: Not use	0x0000_0001
HPF_BYPASS_EN	[0]	RW	Bypass option for internal HPF. 1: bypass 0: pass	0x0000_0000

5.2.1.3.1.7 ECG_CONT

- Base Address: 0x4001_A100
- Address = default_BASE + 0x18, Reset Value = 0x0000_0084

Name	Bit	Type	Description	Reset Value
RLD_EN	[5]	RW	Right Leg Driver(RLD) on/off. 1: enable 0: disable	0x0000_0000
VB_IA_CONT1	[2:0]	RW	ECG channel Common-Mode(VCM) level @ VDD=1.1V 000: 0.33V 001: 0.385V 010: 0.44V 011: 0.495V 100: 0.55V 101: 0.605V 110: 0.66V 111: 0.715V	0x0000_0004

5.2.2 PPG Readout

5.2.2.1 Overview of PPG Measurement

PPG system irradiates light of a particular wavelength to the skin and senses the reflected light which is modulated by the change in blood volume flowing through the capillaries and veins. Following is the basic measurement procedure of PPG:

- Irradiate LEDs synchronized to the AFE sampling sequence.
- Use Photo Diode sensor to detect the reflected light and convert the light signals into photo current.
- Use PPG AFE to convert the photo current signal into voltage and then use an Incremental ADC (IDC) to digitize it.
- Apply the necessary digital signal processing to restore DC level of PPG readout and then calculate the interested health parameter.

The PPG system consists of four transmitters (LED drivers) and two channel of receivers (PPG0, PPG1) as illustrated in *Figure 5-6*. The supply voltage of LED driver is 3 V which is supplied from the pin of AVDD33_LED. The supply voltage of PPG AFE is 3 V which is supplied from the pin of AVDD33A, and the supply voltage of PPG IDC is 2.5 V which is regulated by a built-in regulator. LED driver needs to drive LEDs for the shortest time possible to reduce overall power consumption. S1SBP6A allows LED light controlling time to vary from 50 μs – 2.5 ms with 13-bit register control. Each PPG readout channel consists of a TIA, a sample-and-hold (SNH) stage, and an incremental ADC. The TIA receives photo current from PD. To enlarge dynamic range input photo current in the presence of large ambient light interference, a differential 6 bit current DAC is integrated at the inputs of TIA in each readout channel to cancel out unwanted portions of photo current and restore the DC output level of TIA. Each channel of PPG readout supports 14 noise-free bit conversion when DCC is not in operation. Timing of LED driver is synchronized to that of PPG0, and PPG1 can be used additionally when two PDs are needed.

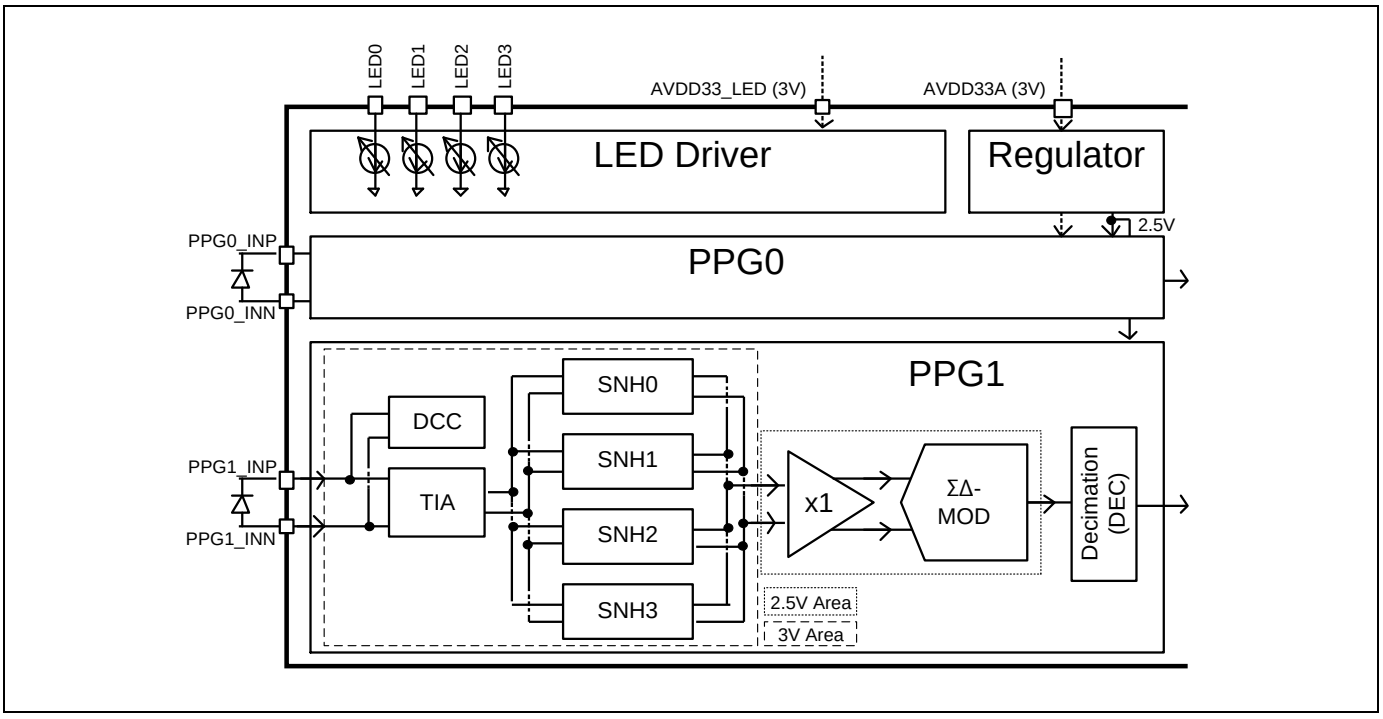


Figure 5-6 Block Diagram for PPG Readout Channel

5.2.2.1.1 PPG System Timing Diagram

The PPG readout front-end has four parallel sample and hold (SNH) paths for each readout channel. As illustrated in *Figure 5-7*, four time slots can be allocated within one pulse repetition period (PPG_PRT). These four time slots can be assigned to the time period of turning on LEDs or the time period for sampling ambient light. For example, you can use two LEDs only within a single period of PPG_PRT. In this case, the slots for LED1 and slots for LED3 can be utilized to sample ambient signals such as AMBIENT1 and AMBIENT2, respectively. You can also use three LEDs within a single period of PPG_PRT. Similarly, AMBIENT3 replaces the slots for LED3 accordingly. Note that the rising edge of PPG sampling clock signal (PPG_SAM[3:0]) delays corresponding LED pulse (LED0, LED1, LED2, or LED3). This delay period encounters LED turn on time and the time required for TIA output sufficiently settling down. In a consequence, correct signal sampling is preceded during High state of PPG_SAM[3:0]. Data conversion process by the IDC stage is then initiated after the PPG_IDCRST goes Low and PPG_CONVT goes High. Finally, 24-bit data is streamed out after PPG_CONVT becomes Low. As illustrated in *Figure 5-7*, when there is no power-down period, after the value of register PPG_EN becomes High, four TIMESLOTs (TIMESLOT0 - TIMESLOT3) are sequentially repeated within a pulse repetition cycle. As illustrated in *Figure 5-8*, the PPG can be powered-down by the state of PPG_IDC_PDN and PPG_AFE_PDN for low-power operation. PPG_PRT and PPG_CONVT determines the time of power-down period. IDLE, TIMESLOTS, TIMELSLOT1-3, TIMESLOTE, and POWERDOWN phase are sequentially repeated within a pulse repetition cycle. The register values of PPG_IDC_PDB_EN and PPG_AFE_PDN_EN enable the power-down option.

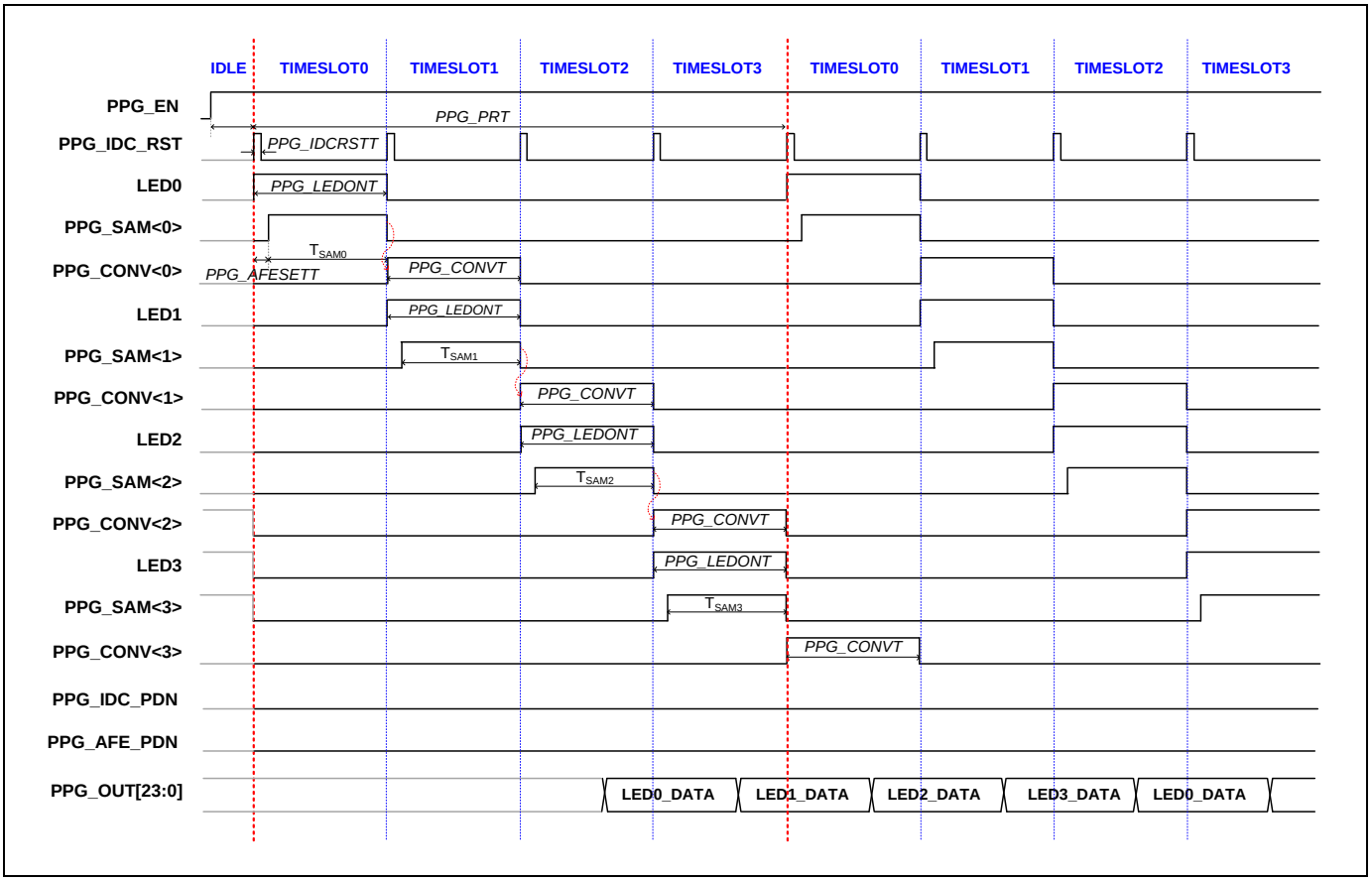


Figure 5-7 Timing Diagram for PPG Readout Channel

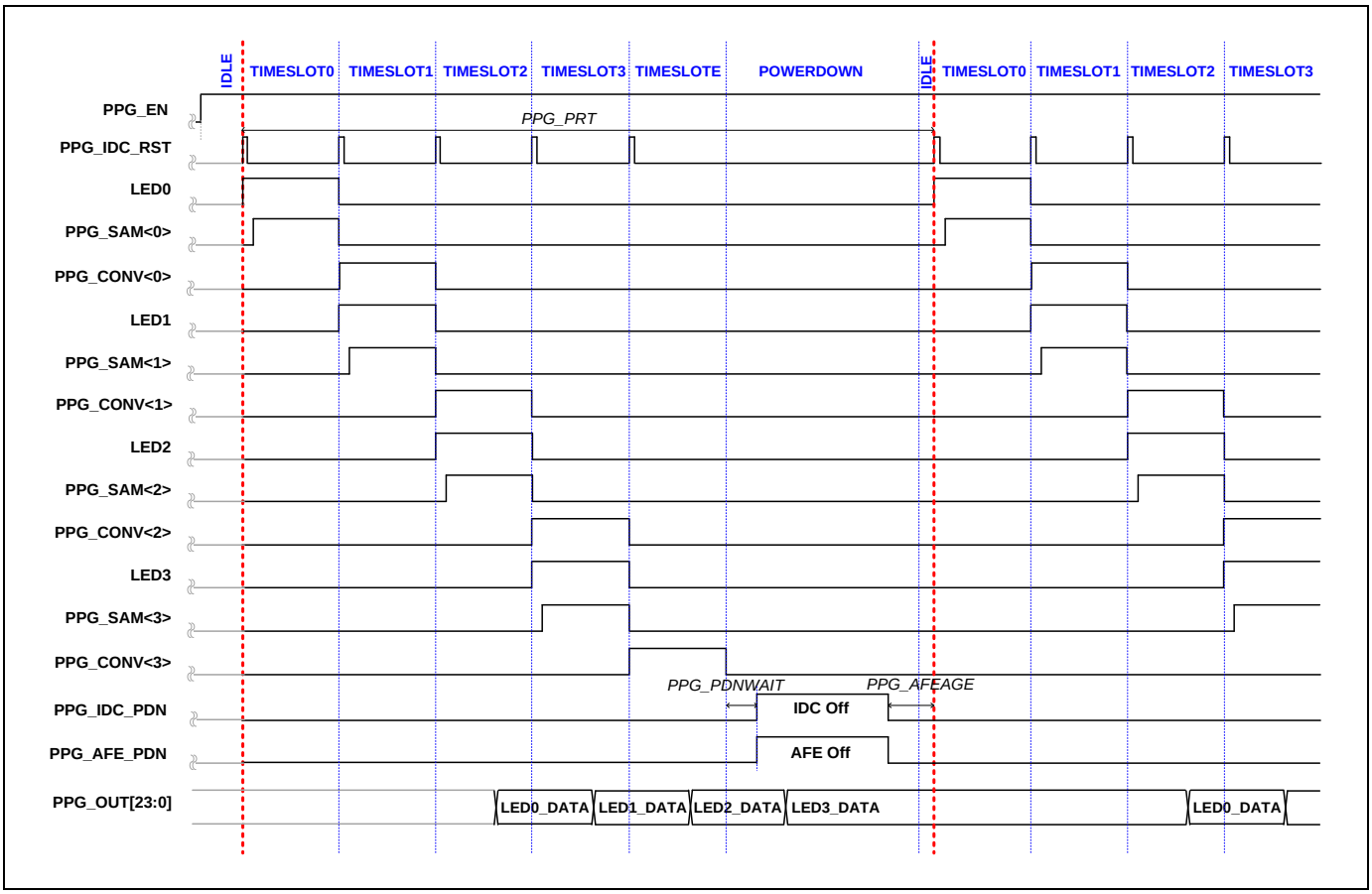


Figure 5-8 Timing Diagram for PPG Readout Channel with Power-Down Period

If PPG_PRT is five times longer than PPG_CONVT, PPG readout front end can be completely turned off to save power consumption. Register settings for timing control are described in *Table 5-1*.

Table 5-1 Timing Controls for PPG

Register	Bit	Default (HEX)	Description
PPG_PRT	17:0	0x1000	PPG Pulse Repetition Time (PRT) control • Pulse repetition time (sec) = PPG_PRT/2.048 MHz • Pulse repetition frequency (Hz) = 2.048 MHz/PPG_PRT Minimum allowable PRT is limited to 1 ms (PPG_PRT = 0x800). Maximum allowable PRT is limited to 10 ms (PPG_PRT = 0x5000).
PPG_LEDONT	12:0	0x00CC	PPG on time control • LED on time (sec) = PPG_LEDONT/2.048 MHz • PPG_LDEONT ≤ PPG_CONVT Maximum allowable LED on time is limited to 2.5 ms (PPG_LEDONT = 0x1400).

5.2.2.2 LED Driver

LED driver is an integrated TX dedicated for PPG readout. The block diagram of LED driver illustrated in *Figure 5-9* consists of the following components:

- Bias block for current DACs. This block generates bias current for current DAC which can change the bias current by controlling the register value of LED_SEL_BIAS.
- Four 7-bit current DACs for two green LEDs, IR LED, and red LED (Current DAC0 and DAC1 are dedicated for driving green LEDs and Current DAC2 and DAC3 are dedicated for driving Red LED or IR LED). Each current DAC supports the options to adjust amount of output current to accommodate to various light intensity requirements of LEDs. Note that output currents of DAC0 ~ DAC3 are separately controlled.
- Digital logic to control LED driver. This logic converts digital signal from controller (LED_CTRLx[6:0] where x denotes 0, 1, 2, or 3, and LED_I_ENLED[3:0]).

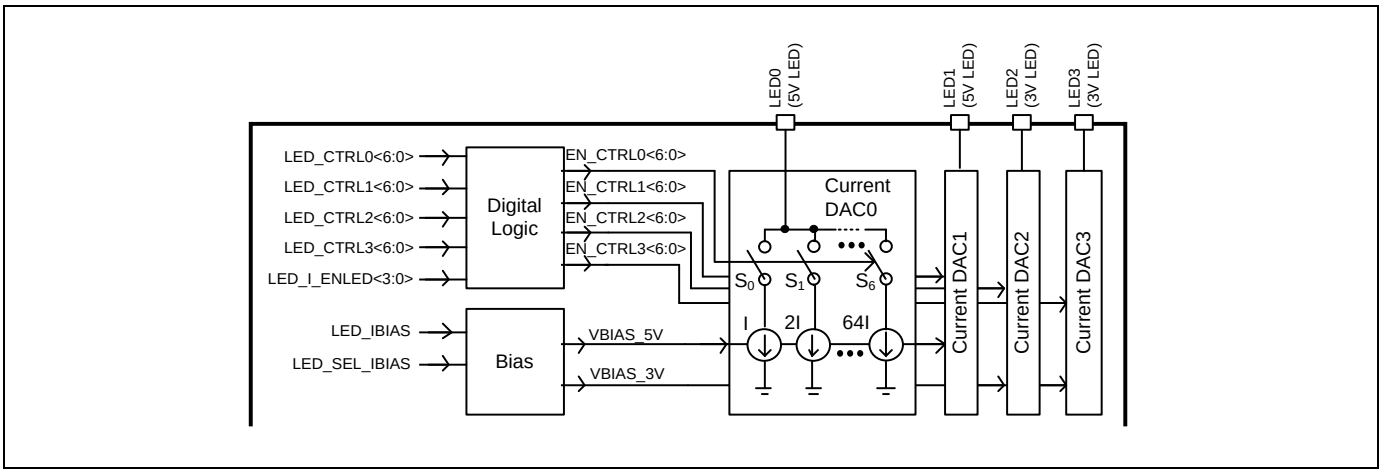


Figure 5-9 Block Diagram of LED Driver

LED driving current is set by the register value of LED_CTRLx, where x can be 0, 1, 2, or 3. Use the following equation to calculate $IDAC_N$.

$$\mathrm{IDAC}_N(\mathrm{a}) = \frac{0.05 \times (2 - \mathrm{LED\_SEL\_BIAS})}{128} \times \mathrm{CTRL}_N$$

Where, $CTRL_N$ is the register value of LED_CTRLx. The minimum value of $IDAC_N$ is determined by the register value of LED_SEL_BIAS as described in *Table 5-2*.

Table 5-2 Minimum Value of Current DAC

LED_SEL_BIAS	Current DAC (mA/step)
0	0.78
1	0.39

Table 5-1 determines the register value of PPG_LEDONT that determines LED on time.

5.2.2.3 PPG Readout Front-End

Two channels of PPG readout are integrated in S1SBP6A. The PPG readout signal chain illustrated in *Figure 5-10* consists of the following components:

- Input switch matrix support the following functions:
  - PPG input short function to measure TIA offset
  - DCC current test
  - TIA reset function to initialize TIA feedback capacitors
- TIA provides variable gain (trans-impedance) and bandwidth. The range of gain is 10 kΩ to 2 MΩ with 3-bit register control. TIA supports a maximum of 100 pF of photo diode junction capacitance.
- Four SNHs integrated in each PPG channel allow separating signals such as RED, RED_AMBIENT, IR, IR_AMBIENT in analog domain. SNH provides low-pass filter function which has the bandwidth range of 40 - 500 Hz depending on the IDC data rate.
- DCC block for current sinking/sourcing at inputs of TIA. Maximum output current of DCC is 16 μA with 6-bit register control in 250 nA/step. This feature enlarges the input dynamic range. Note that DCC current DAC at TIA inputs introduce additional noise to the complete PPG readout. For example, current noise of 100 pA_{rms} RTI (at 0.5 - 20 Hz, TIA gain is 500 kΩ) is evaluated by sourcing/sinking DCC with 8 μA. However, if the DCC current level is increased to 16 μA, the noise is doubled to 200 pA_{rms}.
- Shield driver is integrated to provide shielding external PPG inputs such as PCB input patterns. This feature minimizes the potential capacitive leakage happening at the pins of PPG_INP and PPG_INN.

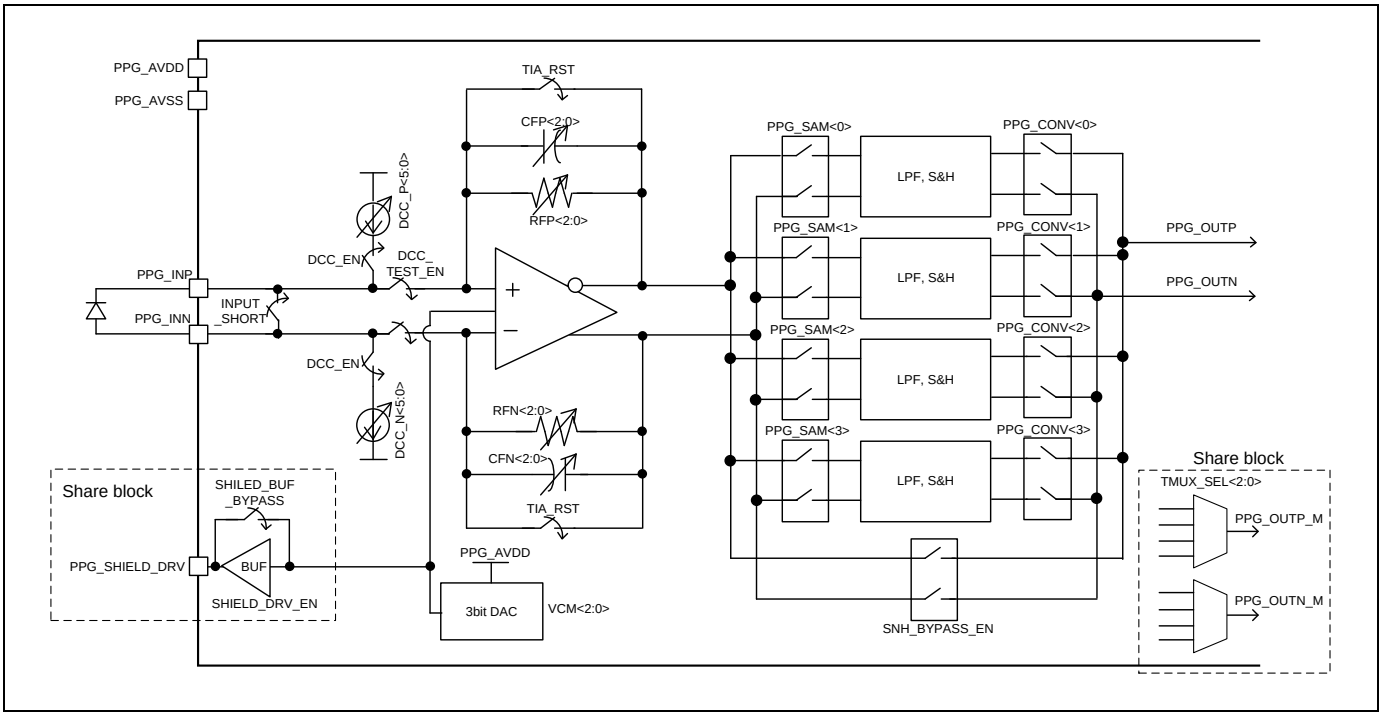


Figure 5-10 Block Diagram of PPG Readout Front-End

5.2.2.3.1 TIA Gain Settings

Programmed value of RFP[2:0] and RFN[2:0] (the feedback resistor of the TIA) sets the value of TIA gain. The register value of PPG_RFP[2:0] and PPG_RFN[2:0] controls the RFP and RFN settings.

5.2.2.3.2 TIA Bandwidth Settings

TIA bandwidth settings are similar to TIA gain settings. The TIA bandwidth is set by programming the value of CFP[2:0] and CFN[2:0] (the feedback capacitance of the TIA). The product of RF and CF gives the time constant of the TIA and must be set approximately 20 % (or less) of the LED or sampling pulse durations. This choice of time constant allows the TIA to effectively pass the incoming pulses from the PD. The register value of PPG_CFP[2:0] and PPG_CFN[2:0] controls CF.

5.2.2.4 Incremental ADC with Digital Decimation

5.2.2.4.1 Overview

IDC is integrated to support PPG AFE. The IDC incorporates voltage buffers at inputs helping to interface with high impedance sensors. The IDC operates with 3 V supply voltage (from the pin of AVDD33A) with internal voltage regulation, and outputs 24-bit data stream at a rate of 4 kSPS. The block diagram of IDC signal chain illustrated in *Figure 5-11* consists of the following components:

- Built-in voltage regulator generates on-chip supply voltage of 2.5 V from an external 3 V voltage source. For the regulator, 10 μF external capacitor is recommended to filter out excessive noise. Optionally, the regulator can be turned-off and IDC can be directly supplied from an external voltage source through regulator output.
- Voltage buffer allows high impedance interface. It supports input signal up to 3.4 V_{p-p} with 2.5 V supply voltage and 3.8 V_{p-p} with 3.0 V supply voltage.
- IDC oversamples analog input signal at a rate of 2.048 MHz. A digital filter is embedded to provide variable IDC data rate of 250, 500, 1k, 2k, 4k (default), 8k, and 16 kSPS.

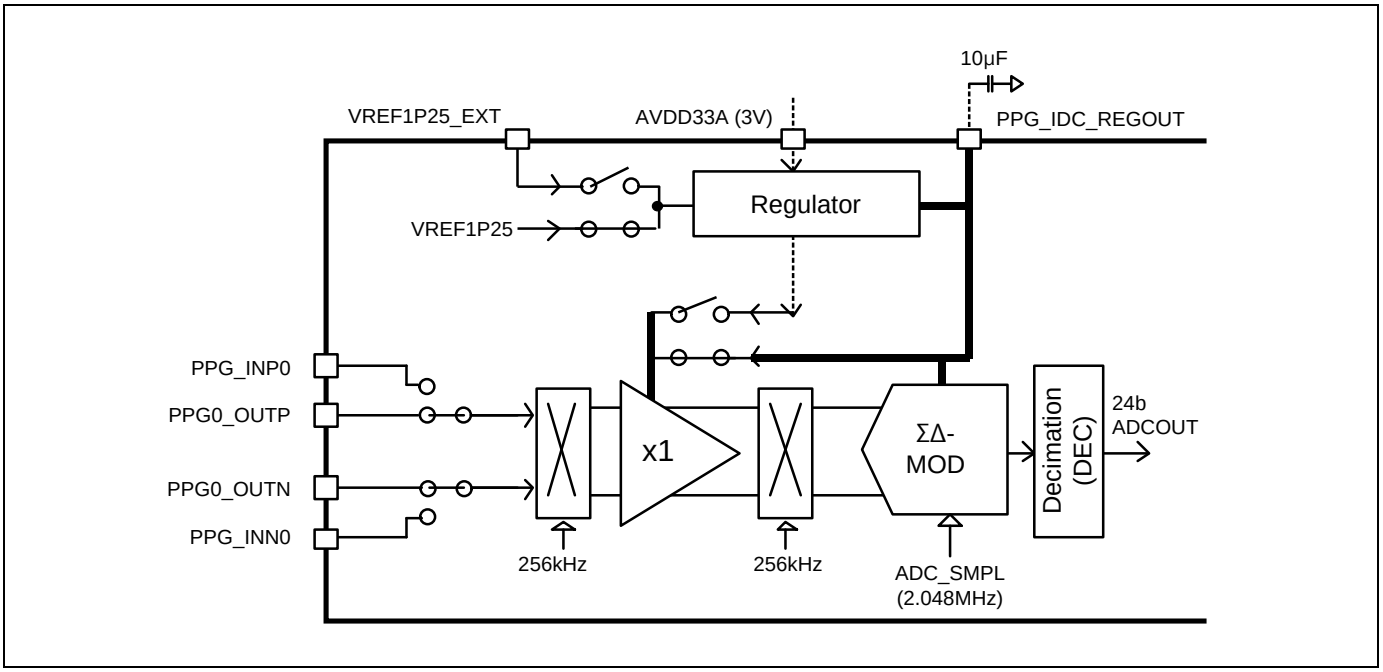


Figure 5-11 Block Diagram of Incremental ADC

5.2.2.4.2 Incremental ADC Control

As illustrated in *Figure 5-12*, IDC samples the input signals and converts them into 24 bit data stream (ADCOUT[23:0]). Sampling frequency of IDC (CLK) is 2.048 MHz and the register value of PPG_CONVT[12:0] adjusts the data rate from 250 SPS to 16 kSPS as described in *Table 5-3.*

Table 5-3 IDC Data Rate Control

PPG_CONVT<12:0>	IDC Data Rate (kSPS)
0000010000000	16
0000100000000	8
0001000000000 (Default)	4 (Default)
0010000000000	2
0100000000000	1
1000000000000	0.5
1111111111111	0.25

Before turning on IDC_EN, ALDO and reference circuits must be turned on and a delay of 4 ms is required for settling down the node of PPG_IDC_REGOUT as illustrated in *Figure 5-11* . IDC should be reset at every conversion. The reset time (Low state of RSTB) is 32 × CLK period (1/2.048 MHz) of ΣΔ MOD.

The IDC has 14-bit current control options such as ICTRL_INT1[3:0], ICTRL_INT2[3:0], ICTRL_INT3[3:0], and ICTRL_QUANT[1:0] that control the current consumption of analog blocks of IDC. The wake up time of IDC (T_{WAKE}) is 50 × CLK period. This time period (PPG_AFEAGE as illustrated in *Figure 5-8*) is required to control PPG_IDC_PDN signal. *Figure 5-12* illustrates the timing diagram of IDC.

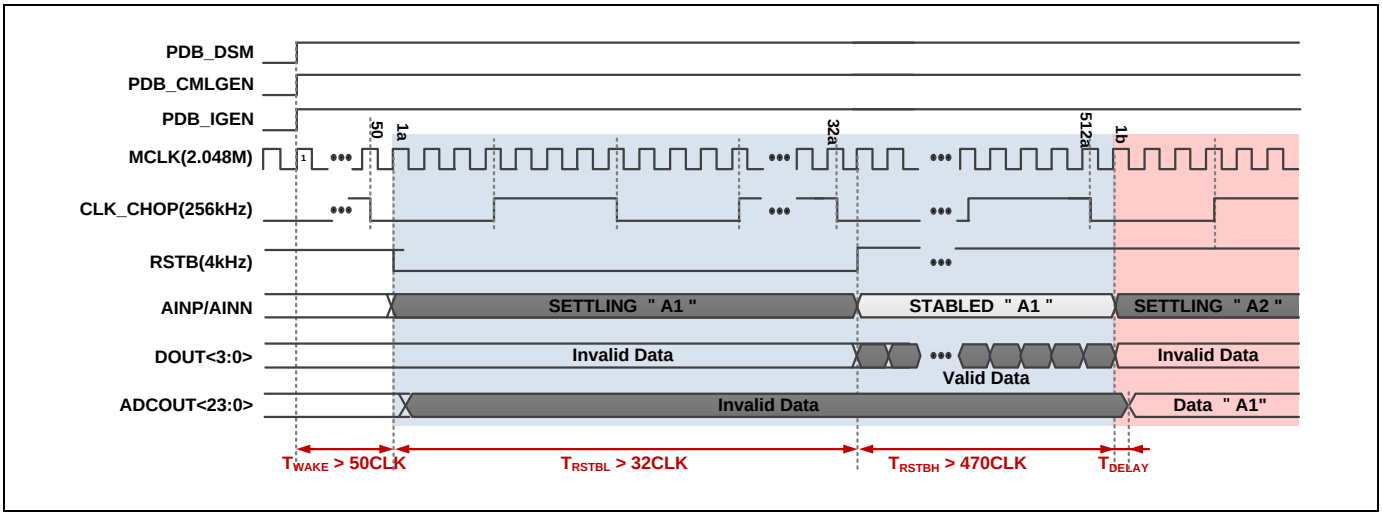


Figure 5-12 Timing Diagram of Incremental ADC

5.2.2.4.3 Digital Filter for Incremental ADC

A decimation filter is required for ΣΔ modulator output to filter out the out-of-band noise from the modulator. Unlike GSR path, where the ΣΔ modulator is followed by SINC filter (consisting of cascade of integrators and differentiators) and FIR filter, only integrators are employed to form decimation filters in IDC.

5.2.2.5 Register Description

This section describes the register map information and its associated registers.

5.2.2.5.1 Register Map Summary

- Base Address: 0x4001_A200

Register	Offset	Description	Reset Value
PPG_GLOBALEN	0x0000	PPG Global Enable	0x0000_0000
PPG0_FUNCEN	0x0004	PPG0 Function Enable	0x0000_09F5
PPG0_TIA	0x0008	PPG0 TIA Control	0x0000_44AD
PPG0_IDC	0x000C	PPG0 IDC Control	0x0085_D666
PPG0_PRT	0x0010	PPG0 PRT Setting	0x0000_1000
PPG0_LEDONT	0x0014	PPG0 LED On-Time Setting	0x0000_00CD
PPG0_LEDTSCTRL	0x0028	PPG0 LED Time Slot Control	0x0000_0005
PPG0_LEDTSCDAC	0x002C	PPG0 LED Current DAC Tiam Slot Control	0x0000_00E4
PPG0_DCCCTRL	0x0030	PPG0 DCC Control	0x0000_0000
PPG1_FUNCEN	0x0044	PPG1 Function Enable	0x0000_09F5
PPG1_TIA	0x0048	PPG1 TIA Control	0x0000_44AD
PPG1_IDC	0x004C	PPG1 IDC Control	0x0085_D666
PPG1_PRT	0x0050	PPG1 PRT Setting	0x0000_1000
PPG1_CONVT	0x0058	PPG1 IDC Conversion Time Setting	0x0001_0200
PPG1_DCCCTRL	0x0070	PPG1 DCC Control	0x0000_0000
PPG_GENERAL	0x0080	PPG General Control	0x0004_0000
LED_FUNCEN	0x00C0	LED Driver Function Enable	0x0000_0000
LED_CDAC0	0x00C8	LED Current DAC0 Control	0x0000_0000
LED_CDAC1	0x00CC	LED Current DAC1 Control	0x0000_0000
LED_CDAC2	0x00D0	LED Current DAC2 Control	0x0000_0000
LED_CDAC3	0x00D4	LED Current DAC3 Control	0x0000_0000

NOTE: If reserved or empty addresses in the register map are changed, S1SBP6A cannot guarantee normal operation.

5.2.2.5.1.1 PPG_GLOBALEN

- Base Address: 0x4001_A200
- Address = Base Address + 0x0000, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
PPG1_AFE_EN	[1]	RW	PPG1 AFE enable. 0: PPG1 AFE disable 1: PPG1 AFE enable	0x0000_0000
PPG0_AFE_EN	[0]	RW	PPG0 AFE enable. 0: PPG0 AFE disable 1: PPG0 AFE enable	0x0000_0000

5.2.2.5.1.2 PPG0_FUNCEN

- Base Address: 0x4001_A200
- Address = Base Address + 0x0004, Reset Value = 0x0000_0860

Name	Bit	Type	Description	Reset Value
PPG0_TIA_EN	[11]	RW	PPG0 TIA control 0: TIA disable 1: TIA enable	0x0000_0001
PPG0_IDC_EN_BUF	[4]	RW	PPG0 BUF enable 0: BUF disable 1: BUF enable	0x0000_0000
PPG0_DCC_EN	[2]	RW	PPG0 DC Cancellation (DCC) enable 0: DCC disable 1: DCC enable	0x0000_0000
PPG0_AFE_PDN_EN	[0]	RW	PPG0 AFE power-down mode enable 0: AFE always-on 1: AFE power down mode enable	0x0000_0000

5.2.2.5.1.3 PPG0_TIA

- Base Address: 0x4001_A200
- Address = Base Address + 0x0008, Reset Value = 0x0000_44AD

Name	Bit	Type	Description	Reset Value
PPG0_TIARST	[15]	RW	PPG0 TIA reset control. 0: Reset release 1: Reset assert	0x0000_0000
PPG0_VCM	[14:12]	RW	PPG0 TIA Vcm control. 000: 1.05 V 001: 1.10 V	0x0000_0004

Name	Bit	Type	Description	Reset Value
			010: 1.15 V 011: 1.20 V 100: 1.25 V 101: 1.30 V 110: 1.35 V 111: 1.40 V	
PPG0_CFN	[11:9]	RW	PPG0 TIA N-path capacitor control. 000: 2 pF 001: 4 pF 010: 6 pF 011: 8 pF 100: 10 pF 101: 14 pF 110: 18 pF 111: 22 pF	0x0000_0002
PPG0_CFP	[8:6]	RW	PPG0 TIA P-path capacitor control. 000: 2 pF 001: 4 pF 010: 6 pF 011: 8 pF 100: 10 pF 101: 14 pF 110: 18 pF 111: 22 pF	0x0000_0002
PPG0_RFN	[5:3]	RW	PPG0 TIA N-path resistor control. 000: 10 kΩ 001: 25 kΩ 010: 50 kΩ 011: 100 kΩ 100: 250 kΩ 101: 500 kΩ 110: 1 MΩ 111: 2 MΩ	0x0000_0005
PPG0_RFP	[2:0]	RW	PPG0 TIA P-path resistor control. 000: 10 kΩ 001: 25 kΩ 010: 50 kΩ 011: 100 kΩ 100: 250 kΩ 101: 500 kΩ 110: 1 MΩ 111: 2 MΩ	0x0000_0005

5.2.2.5.1.4 PPG0_IDC

- Base Address: 0x4001_A200
- Address = Base Address + 0x000C, Reset Value = 0x0080_1666, Default Value = 0x0085_D666

Name	Bit	Type	Description	Reset Value
PPG0_IDC_BUF_CMO_CTRL	[18]	RW	PPG0 Buffer common mode voltage select	0x0000_0000
PPG0_IDC_BUF_I_CTRL	[17:16]	RW	PPG0 Buffer current control	0x0000_0000
PPG0_IDC_BUF_EN_CHOP	[15]	RW	PPG0 Buffer chopping control 0: Buffer chopping disable 1: Buffer chopping enable	0x0000_0000
PPG0_IDC_BUF_PWR_SEL	[14]	RW	PPG0 Buffer power select	0x0000_0000
PPG0_IDC_ICTRL_QUANT	[13:12]	RW	PPG0 IDC quantizer current control	0x0000_0001
PPG0_IDC_ICTRL_INT3	[11:8]	RW	PPG0 IDC current control for integrator 3	0x0000_0006
PPG0_IDC_ICTRL_INT2	[7:4]	RW	PPG0 IDC current control for integrator 2	0x0000_0006
PPG0_IDC_ICTRL_INT1	[3:0]	RW	PPG0 IDC current control for integrator 1	0x0000_0006

5.2.2.5.1.5 PPG0_PRT

- Base Address: 0x4001_A200
- Address = Base Address + 0x0010, Reset Value = 0x0000_5000

Name	Bit	Type	Description	Reset Value
PPG0_PRT	[17:0]	RW	PPG0 pulse repetition time (PRT) control. *Pulse repetition time (sec) = PPG0_PRT / 2.048 MHz *Pulse repetition frequency (Hz) = 2.048 MHz / PPG0_PRT Minimum allowable PRT is limited to 1 ms (PPG0_PRT = 0x800) and maximum allowable PRT is limited to 10 ms (PPG0_PRT = 0x5000).	0x0000_1000

5.2.2.5.1.6 PPG0_LEDONT

- Base Address: 0x4001_A200
- Address = Base Address + 0x0014, Reset Value = 0x0000_00CD

Name	Bit	Type	Description	Reset Value
PPG0_LEDONT	[12:0]	RW	PPG0 LED on-time control. *LED on-time (sec) = PPG0_LEDONT / 2.048 MHz Maximum allowable LED on-time is limited to 2.5 ms (PPG0_LEDONT = 0x1400).	0x0000_00CD

5.2.2.5.1.7 PPG0_LEDTSCTRL

- Base Address: 0x4001_A200
- Address = Base Address + 0x0028, Reset Value = 0x0000_0005

Name	Bit	Type	Description	Reset Value
PPG0_LEDDCTS3	[7]	RW	PPG0 LED DC control enable for Time Slot 3 0: LED DC control disable for Time Slot 3 1: LED DC control enable for Time Slot 3	0x0000_0000
PPG0_LEDDCTS2	[6]	RW	PPG0 LED DC control enable for Time Slot 2 0: LED DC control disable for Time Slot 2 1: LED DC control enable for Time Slot 2	0x0000_0000
PPG0_LEDDCTS1	[5]	RW	PPG0 LED DC control enable for Time Slot 1 0: LED DC control disable for Time Slot 1 1: LED DC control enable for Time Slot 1	0x0000_0000
PPG0_LEDDCTS0	[4]	RW	PPG0 LED DC control enable for Time Slot 0 0: LED DC control disable for Time Slot 0 1: LED DC control enable for Time Slot 0	0x0000_0000
PPG0_LEDENTS3	[3]	RW	PPG0 LED enable for Time Slot 3 0: LED disable for Time Slot 3 1: LED enable for Time Slot 3	0x0000_0000
PPG0_LEDENTS2	[2]	RW	PPG0 LED enable for Time Slot 2 0: LED disable for Time Slot 2	0x0000_0001

			1: LED enable for Time Slot 2	
PPG0_LEDENTS1	[1]	RW	PPG0 LED enable for Time Slot 1 0: LED disable for Time Slot 1 1: LED enable for Time Slot 1	0x0000_0000
PPG0_LEDENTS0	[0]	RW	PPG0 LED enable for Time Slot 0 0: LED disable for Time Slot 0 1: LED enable for Time Slot 0	0x0000_0001

5.2.2.5.1.8 PPG0_LEDTSCDAC

- Base Address: 0x4001_A200
- Address = Base Address + 0x002C, Reset Value = 0x0000_00E4

Name	Bit	Type	Description	Reset Value
PPG0_TSSELCDAC3	[7:6]	RW	LED Current DAC3 Time Slot select. 00: Time Slot 0 01: Time Slot 1 10: Time Slot 2 11: Time Slot 3	0x0000_0003
PPG0_TSSELCDAC2	[5:4]	RW	LED Current DAC2 Time Slot select. 00: Time Slot 0 01: Time Slot 1 10: Time Slot 2 11: Time Slot 3	0x0000_0002
PPG0_TSSELCDAC1	[3:2]	RW	LED Current DAC1 Time Slot select. 00: Time Slot 0 01: Time Slot 1 10: Time Slot 2 11: Time Slot 3	0x0000_0001
PPG0_TSSELCDAC0	[1:0]	RW	LED Current DAC0 Time Slot select. 00: Time Slot 0 01: Time Slot 1 10: Time Slot 2 11: Time Slot 3	0x0000_0000

5.2.2.5.1.9 PPG0_DCCCTRL

- Base Address: 0x4001_A200
- Address = Base Address + 0x0030, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
PPG0_DCCN	[11:6]	RW	PPG0 DC cancellation control for N path.	0x0000_0000
PPG0_DCCP	[5:0]	RW	PPG0 DC cancellation control for P path.	0x0000_0000

5.2.2.5.1.10 PPG1_FUNCEN

- Base Address: 0x4001_A200
- Address = Base Address + 0x0044, Reset Value = 0x0000_0860

Name	Bit	Type	Description	Reset Value
PPG1_TIA_EN	[11]	RW	PPG1 TIA control. 0: TIA disable 1: TIA enable	0x0000_0001
PPG1_IDC_BUF_BYPASS	[9]	RW	PPG1 BUF bypass control. 0: Pass 1: Bypass	0x0000_0000
PPG1_IDC_PDB_EN	[8]	RW	PPG1 IDC power down mode control. 0: IDC power down mode disable 1: IDC power down mode enable	0x0000_0001
PPG1_IDC_EN	[7]	RW	PPG1 IDC enable. 0: IDC disable 1: IDC enable	0x0000_0000
PPG1_IDC_EN_CHOP	[5]	RW	PPG1 IDC chopping enable. 0: Chopping mode disable 1: Chopping mode enable	0x0000_0001
PPG1_IDC_EN_BUF	[4]	RW	PPG1 BUF enable. 0: BUF disable 1: BUF enable	0x0000_0000
PPG1_DCC_EN	[2]	RW	PPG1 DC Cancellation (DCC) enable. 0: DCC disable 1: DCC enable	0x0000_0000

5.2.2.5.1.11 PPG1_TIA

- Base Address: 0x4001_A200
- Address = Base Address + 0x0048, Reset Value = 0x0000_44AD

Name	Bit	Type	Description	Reset Value
PPG1_TIARST	[15]	RW	PPG1 TIA reset control. 0: Reset release 1: Reset assert	0x0000_0000
PPG1_VCM	[14:12]	RW	PPG1 TIA Vcm control. 000: 1.05 V 001: 1.10 V 010: 1.15 V 011: 1.20 V 100: 1.25 V 101: 1.30 V 110: 1.35 V 111: 1.40 V	0x0000_0004
PPG1_CFN	[11:9]	RW	PPG1 TIA N-path capacitor control. 000: 2 pF 001: 4 pF 010: 6 pF 011: 8 pF 100: 10 pF 101: 14 pF 110: 18 pF 111: 22 pF	0x0000_0002
PPG1_CFP	[8:6]	RW	PPG1 TIA P-path capacitor control. 000: 2 pF 001: 4 pF 010: 6 pF 011: 8 pF 100: 10 pF 101: 14 pF 110: 18 pF 111: 22 pF	0x0000_0002
PPG1_RFN	[5:3]	RW	PPG1 TIA N-path resistor control. 000: 10 kΩ 001: 25 kΩ 010: 50 kΩ 011: 100 kΩ 100: 250 kΩ 101: 500 kΩ 110: 1 MΩ 111: 2 MΩ	0x0000_0005

Name	Bit	Type	Description	Reset Value
PPG1_RFP	[2:0]	RW	PPG1 TIA P-path resistor control. 000: 10 kΩ 001: 25 kΩ 010: 50 kΩ 011: 100 kΩ 100: 250 kΩ 101: 500 kΩ 110: 1 MΩ 111: 2 MΩ	0x0000_0005

5.2.2.5.1.12 PPG1_IDC

- Base Address: 0x4001_A200
- Address = Base Address + 0x004C, Reset Value = 0x0080_1666, Default Value = 0x0085_D666

Name	Bit	Type	Description	Reset Value
PPG1_IDC_BUF_CMO_CTRL	[18]	RW	PPG1 Buffer common mode voltage select.	0x0000_0000
PPG1_IDC_BUF_I_CTRL	[17:16]	RW	PPG1 Buffer current control.	0x0000_0000
PPG1_IDC_BUF_EN_CHOP	[15]	RW	PPG1 Buffer chopping control. 0: Buffer chopping disable 1: Buffer chopping enable	0x0000_0000
PPG1_IDC_BUF_PWR_SEL	[14]	RW	PPG1 Buffer power select.	0x0000_0000
PPG1_IDC_ICTRL_QUANT	[13:12]	RW	PPG1 IDC quantizer current control.	0x0000_0001
PPG1_IDC_ICTRL_INT3	[11:8]	RW	PPG1 IDC current control for integrator 3.	0x0000_0006
PPG1_IDC_ICTRL_INT2	[7:4]	RW	PPG1 IDC current control for integrator 2.	0x0000_0006
PPG1_IDC_ICTRL_INT1	[3:0]	RW	PPG1 IDC current control for integrator 1.	0x0000_0006

5.2.2.5.1.13 PPG1_PRT

- Base Address: 0x4001_A200
- Address = Base Address + 0x0050, Reset Value = 0x0000_5000

Name	Bit	Type	Description	Reset Value
PPG1_PRT	[17:0]	RW	PPG1 pulse repetition time (PRT) control. *Pulse repetition time (sec) = PPG1_PRT / 2.048 MHz *Pulse repetition	0x0000_1000

			frequency (Hz) = 2.048 MHz / PPG1_PRT Minimum allowable PRT is limited to 1 ms (PPG1_PRT = 0x800) and maximum allowable PRT is limited to 10 ms (PPG1_PRT = 0x5000).	

5.2.2.5.1.14 PPG1_DCCCTRL

- Base Address: 0x4001_A200
- Address = Base Address + 0x0070, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
PPG1_DCCN	[11:6]	RW	PPG1 DC cancellation control for N path.	0x0000_0000
PPG1_DCCP	[5:0]	RW	PPG1 DC cancellation control for P path.	0x0000_0000

5.2.2.5.1.15 PPG_GENERAL

- Base Address: 0x4001_A200
- Address = Base Address + 0x0080, Reset Value = 0x0004_0000

Name	Bit	Type	Description	Reset Value
PPG_LED_DCC_SYNC	[19]	RW	Synchronize DCC control with LED turn on timing for test purpose. 0: Disable 1: Enable	0x0000_0000
PPG_IDC_CLK_DLY	[18]	RW	PPG IDC clock delay control by 90 degrees between IDC0 and IDC1. 0: No delay 1: Delay by 90 degrees	0x0000_0001
PPG_TMUXSEL	[13:11]	RW	PPG AFE analog signal select to monitor.	0x0000_0000
PPG_IDC_EN_LDO	[2]	RW	PPG LDO enable. 0: PPG LDO disable 1: PPG LDO enable	0x0000_0001
PPG_SHIELD_DRV_EN	[1]	RW	PPG Shield Driver enable. 0: Shield Driver disable 1: Shield Driver enable	0x0000_0001
PPG_SHIELD_BUF_BYPASS	[0]	RW	PPG Shield Buffer bypass enable. 0: Shield Buffer bypass disable 1: Shield Buffer bypass enable	0x0000_0000

5.2.2.5.1.16 LED_FUNCEN

- Base Address: 0x4001_A200
- Address = Base Address + 0x00C0, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
LED_SEL_IBIAS	[1]	RW	LED Driver bias current select. 0: Current steps of 0.8 mA 1: Current steps of 0.4 mA	0x0000_0000
LED_EN	[0]	RW	LED Driver global enable. 0: LED Driver global disable 1: LED Driver global enable	0x0000_0000

5.2.2.5.1.17 LED_CDAC0

- Base Address: 0x4001_A200
- Address = Base Address + 0x00C8, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
LED_CDAC0	[6:0]	RW	LED Driver Current DAC0 (5 V device) control. Min.: 0 mA Max.: 100 mA	0x0000_0000

5.2.2.5.1.18 LED_CDAC1

- Base Address: 0x4001_A200
- Address = Base Address + 0x00CC, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
LED_CDAC1	[6:0]	RW	LED Driver Current DAC0 (5 V device) control. Min.: 0 Ma Max.: 100 mA	0x0000_0000

5.2.2.5.1.19 LED_CDAC2

- Base Address: 0x4001_A200
- Address = Base Address + 0x00D0, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
LED_CDAC2	[6:0]	RW	LED Driver Current DAC0 (3 V device) control. Min.: 0 mA Max. 100 mA	0x0000_0000

5.2.2.5.1.20 LED_CDAC3

- Base Address: 0x4001_A200
- Address = Base Address + 0x00D4, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
LED_CDAC3	[6:0]	RW	LED Driver Current DAC0 (3 V device) control. Min.: 0 mA Max.: 100 mA	0x0000_0000

5.2.3 BIA Readout

5.2.3.1 Overview

The BIA applied in S1SBP6A measures the impedance of body to estimate the body fat and body composition. The BIA applies sinusoidal current signals into the body through a pair of electrodes to measure the body composition. BIA readout uses another pair of electrodes to measure voltage signals generated across the impedance level of body. The supply voltage of BIA readout is 1.1 V and the built-in ALDO regulates it. The BIA readout consists of the following components:

- A Direct Digital Synthesizer (DDS) and 6-bit DAC to generate the sinusoidal voltage signal.
- A current driver to apply the generated sinusoidal current signal into the body.
- A built-in input and output switch fabric to select the switches connected to calibration networks or body measuring circuits.
- An input PGA stage to provide additional signal amplification of from 1x to 3x.
- A built-in input HPF to avoid DC offset amplification.
- A clock generation circuits to supply clock signals for Rectify mode.
- An output PGA stage to provide additional signal amplification of from 0.5x to 4x.
- A 12-bit ADC for BIA signal digitization. This ADC can be operated at a rate of either 1 kSPS or 8 kSPS with integrated digital decimation filter to provide improved ENOB.

Figure 5-13 illustrates the block diagram of BIA readout.

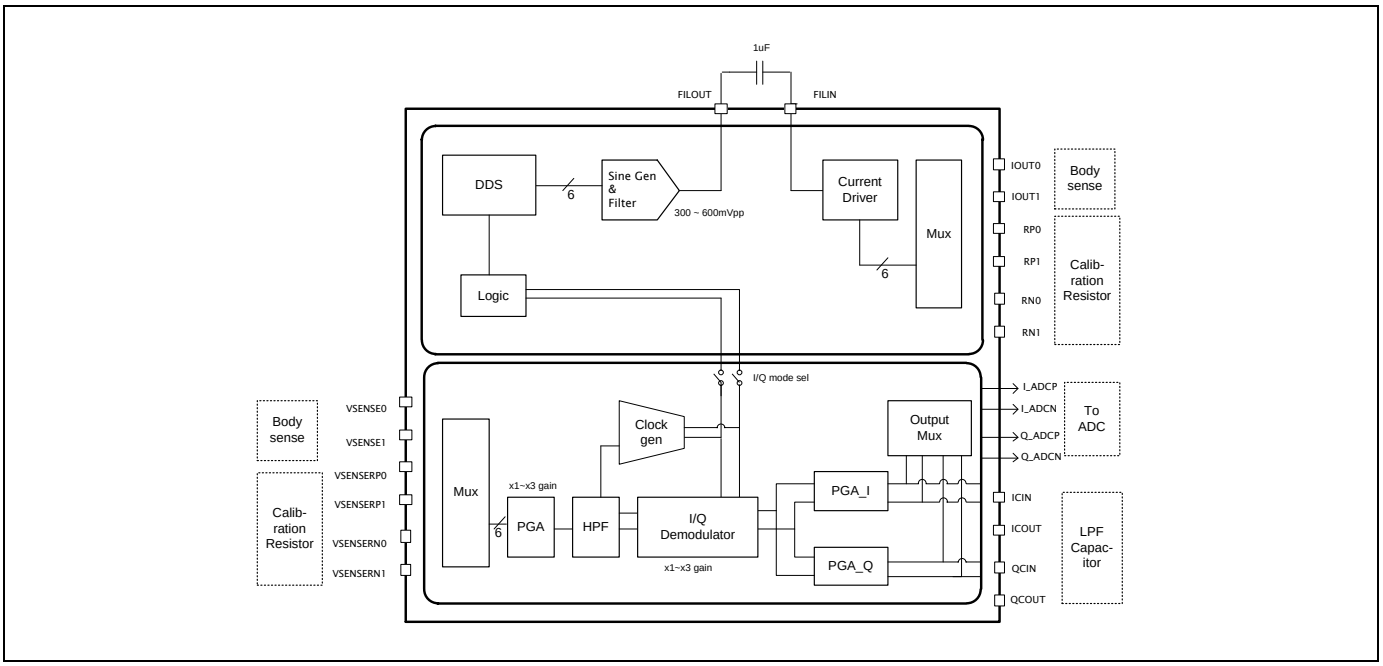


Figure 5-13 Block Diagram of BIA Readout

5.2.3.2 Functional Description

You can measure the impedance of the body to calculate the composition and match the result in a table with specified body fat calculation algorithm. The algorithm is usually based on age, sex, weight, and so on. The block diagram of BIA readout illustrated in *Figure 5-13* consists of a sinusoidal current driver as TX and voltage readout as RX. The TX injects current signal whose frequency and the shape of wave are determined by DDS. This current signal modulates impedance of body into voltage signal. Then, RX amplifies the voltage signal at the input PGA and then uses either rectify or I/Q mode to demodulate the signal.

In the TX, DDS generates 6-bit signals for the voltage DAC to create sinusoidal analog signal which has programmable frequency ranging from 1 kHz to 1 MHz. LPF filters the DAC output. The result is then AC coupled by an external capacitor to restore signal common mode. Finally, an output driver converts it into current signal.

- **Rectify-Mode**

In the Rectify-mode illustrated in *Figure 5-14*, the readout channel uses self-generated clock signal to perform full wave rectification. The rectified signal is low-pass filtered and used as an input to 12-bit ADC. The LPF uses external large capacitors at its output pins. It is recommended to use one of the several μF capacitors to sufficiently remove the ripples of the demodulation signal.

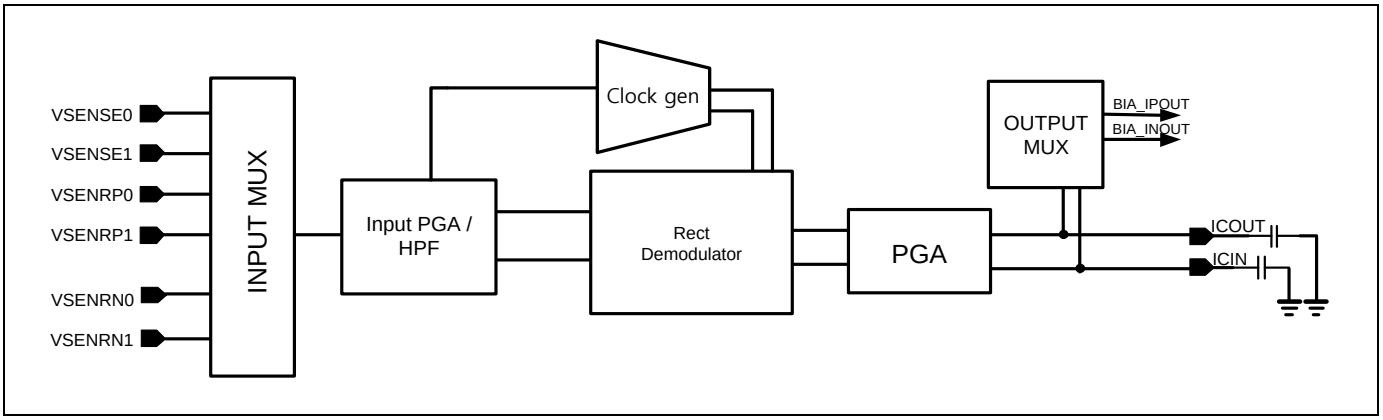


Figure 5-14 Block Diagram of BIA Rectify Mode

5.2.3.3 Register Description

This section describes the register map information and its associated registers.

5.2.3.3.1 Register Map Summary

- Base Address: 0x4001_A300

Register	Offset	Description	Reset Value
BIA_TX_FIL	0x0000	TX Filter -3dB Frequency	0x0000_0001
BIA_TX_FREQ	0x0004	TX Drive Frequency	0x0000_0032
BIA_TX_AMPL	0x0008	TX DAC Output Amplitude	0x0000_00A0
BIA_TX_CUR	0x000C	TX Current Set	0x0000_0000
BIA_TX_SW	0x0010	TX Output Software Mux Set	0x0000_0001
BIA_RX_INPUT	0x0014	RX Input Software Mux Set	0x0000_0000
BIA_RX_AMP1	0x0018	RX Amp Gain, Mode Select	0x0000_0001
BIA_RX_AMP2	0x001C	RX I/Q Amp Gain Set	0x0000_0033
BIA_RX_FIL	0x0020	Output LPF Frequency Set	0x0000_0002
BIA_RX_AMP3	0x0024	RX DC Amp Gain, RX Current Set	0x0000_0034
BIA_RX_COMP	0x0028	RX COMP Amp Control	0x0000_0049
BIA_IQ_GEN	0x003C	IQ Mode Clock Control	0x0000_0003
BIA_TRX_EN	0x0048	TX RX Enable	0x0000_0000
BIA_HPF_EN	0x0058	HPF Enable	0x0000_0001

NOTE: If reserved or empty addresses in the register map are changed, S1SBP6A cannot guarantee normal operation.

5.2.3.3.1.1 BIA_TX_FIL

- Base Address: 0x4001_A300
- Address = Base Address + 0x0000, Reset Value = 0x0000_0001

Name	Bit	Type	Description	Reset Value
RSVD0	[7:2]	RW	Reserved	0x0000_0000
BIAFIL	[1:0]	RW	* DAC output LPF 3dB control. 00: 125 kHz 01 : 500 kHz 10 : 1000 kHz 11 : 2000 kHz	0x0000_0001

5.2.3.3.1.2 BIA_TX_FREQ

- Base Address: 0x4001_A300
- Address = Base Address + 0x0004, Reset Value = 0x0000_0032

Name	Bit	Type	Description	Reset Value
DACFREQ_0	[9:0]	RW	* DDS Frequency Selection. - DAC output frequency = DACFREQ<9:0> * Fclk / 4096, For example with Fclk=4 MHz , FF = 1 MHz	0x0000_0032

5.2.3.3.1.3 BIA_TX_AMPL

- Base Address: 0x4001_A300
- Address = Base Address + 0x0008, Reset Value = 0x0000_00A0

Name	Bit	Type	Description	Reset Value
DACI	[7:6]	RW	* DAC output voltage range setting. 00 : 300 mV 01 : 400 mV 10 : 500 mV 11 : 600 mV	0x0000_0002
DAC	[5:0]	RW	* DAC output voltage control by code.	0x0000_0020

5.2.3.3.1.4 BIA_TX_CUR

- Base Address: 0x4001_A300
- Address = Base Address + 0x000C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD0	[7:4]	RW	Reserved	0x0000_0000
IDUP	[3]	RW	* Increase a driving current when 1.	0x0000_0000
ICONT	[2]	RW	* TX amp current increase when 1.	0x0000_0000
ITOPUP	[1]	RW	* TX top current up if needed.	0x0000_0000
IAMPUP	[0]	RW	* TX drive amp current increase when 1.	0x0000_0000

5.2.3.3.1.5 BIA_TX_SW

- Base Address: 0x4001_A300
- Address = Base Address + 0x0010, Reset Value = 0x0000_0001

Name	Bit	Type	Description	Reset Value
RSVD0	[7:6]	RW	Reserved	0x0000_0000
DACSRN	[5:4]	RW	*TX output switches control. 00 : NA 01 : RN0 10 : RN1 11 : NA	0x0000_0000
DACSRP	[3:2]	RW	*TX output switches control. 00 : NA 01 : RP0 10 : RP1 11: NA	0x0000_0000
DACSI	[1:0]	RW	* TX output switches control. 00 : NA 01 : Body measure 10 : NA 11 : NA	0x0000_0001

5.2.3.3.1.6 BIA_RX_INPUT

- Base Address: 0x4001_A300
- Address = Base Address + 0x0014, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD0	[7:4]	RW	Reserved	0x0000_0000
VSENCTRP	[3:2]	RW	* Read Channel P input signal control. 00 : Body impedance 01 : Body impedance reverse direction 10 : Outer resistor0 11 : Outer resistor1	0x0000_0000
VSENCTRN	[1:0]	RW	* Read Channel N input signal control. 00 : Body impedance 01 : Body impedance reverse direction 10 : Outer resistor0 11 : Outer resistor1	0x0000_0000

5.2.3.3.1.7 BIA_RX_AMP1

- Base Address: 0x4001_A300
- Address = Base Address + 0x0018, Reset Value = 0x0000_0001

Name	Bit	Type	Description	Reset Value
RSVD0	[7:5]	RW	Reserved	0x0000_0000
RSVD1	[3]	RW	Reserved	0x0000_0000
AMPCTRL	[2:0]	RW	* BIA input buffer Amp. Gain control. 000 : x0.5 001 : x1.0 011 : x2.0 111 : NA	0x0000_0001

5.2.3.3.1.8 BIA_TRX_EN

- Base Address: 0x4001_A300
- Address = Base Address + 0x0048, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
BIA_RX_EN	[1]	RW	Enable BIA RX.	0x0000_0000
BIA_TX_EN	[0]	RW	Enable BIA TX.	0x0000_0000

5.2.3.3.1.9 BIA_HPF_EN

- Base Address: 0x4001_A300
- Address = Base Address + 0x0058, Reset Value = 0x0000_0001

Name	Bit	Type	Description	Reset Value
BIA_HPF_EN	[0]	RW	HPF enable 0: HPF off 1: HPF on	0x0000_0001

5.2.4 GP Analog Interfaces

5.2.4.1 12-bit Analog Readout (GP Analog0/1)

12-bit analog readout front-end, as illustrated in *Figure 5-15*, is integrated to support versatile sensor interface applications where low-power and medium-range resolution is the primary concern. Prior to ADC, highly flexible AFEs are embedded. They are grouped into two in which General Purpose (GP) Analog0 functions as a Variable Gain Amplifier (VGA), a Trans-Impedance Amplifier (TIA), or a LPF, and GP Analog1 behaves as a voltage attenuator and a die temperature sensor. The flexibilities of GP Analog 0/1 are realized by integrated switch matrix and you can easily program them based on the preference. The outputs of GP Analog 0/1 are digitized by a 12-bit ADC operating at a rate of 1 kSPS or 8 kSPS in a time-multiplexed manner.

- LPF in GP Analog0 provides first-order differential mode bandwidth from 1 kHz to 16.3 kHz.
- Voltage attenuator supports input voltage signals up to 1.4 V_{p-p} with attenuation of 1/5 (For example, Rext = 200 kΩ). Note that resistor of 100 kΩ is internally integrated.
- ADC for GP Analog0/1 operates at a rate of either 1 kSPS or 8 kSPS and it outputs 12-bit digital code.

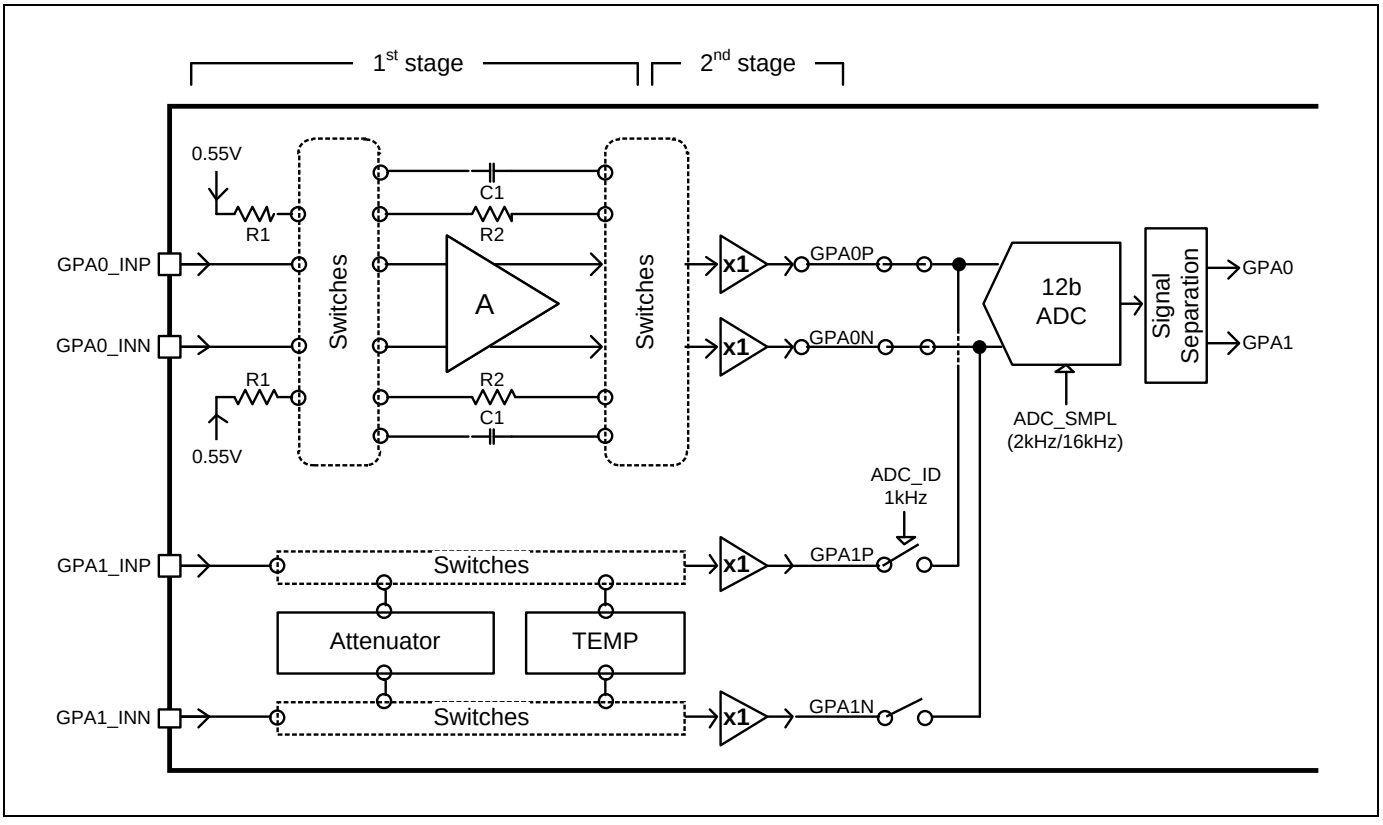


Figure 5-15 Block Diagram of 12-bit Analog Readout

5.2.4.1.1 Switch Configurations for GP Analog0

GP Analog0 Integrates 12 switches which can be configured by the register value of GPA0_SW_SEL[11:0]. *Table 5-4* describes the detail switch configurations in GP Analog0.

Table 5-4 Switch Configurations in GP Analog0

Stage	Interface	GPA0_SW_SEL[11:0]											
		11	10	9	8	7	6	5	4	3	2	1	0
1st stage	TIA	–	–	0	0	1	1	1	1	0	1	1	0
	VGA	–	–	0	0	1	1	1	1	1	0	0	1
	LPF	–	–	0	1	1	0	0	1	0	1	1	0
	Bypass (1st-stage)	–	–	1	0	0	0	0	0	0	0	0	0
2nd stage	ADC Driver	1	0	–	–	–	–	–	–	–	–	–	–
	Bypass (2nd-stage)	0	1	–	–	–	–	–	–	–	–	–	–

5.2.4.1.1.1 TIA in GP Analog0

For TIA configuration illustrated in *Figure 5-16*, GPA0_INP/INN can receive differential current signal (for example, from Photo Diode). The TIA provides differential trans-impedance gain of 2 x R2. The value of R2 can be adjusted in five steps according to the register value of GPA0_R2_CTRL[1:0] and GPA0_R2_300K. The TIA also equips capacitor C1 in parallel with R2. This arrangement can provide first-order anti-alias filter for the ADC. In addition, C1 helps to compensate for the stability when there is pronounced capacitance presented at inputs. The value of C1 can be configured in four steps according to the register value of GPA0_C1_CTRL[1:0], and it provides wide range of -3 dB bandwidth depending on the value of R2. Internally, the TIA output is biased to the half of ADC reference voltage, 0.55 V. Use the following equations to determine the gain and bandwidth of TIA.

$$\mathbf{Gain}\ (\mathbf{V/A}) = \mathbf{2 \cdot R_2}$$

$$\mathbf{Bandwidth}\ (\mathbf{Hz}) = \frac{\mathbf{1}}{\mathbf{2 \cdot \pi \cdot R_2 \cdot C_1}}$$

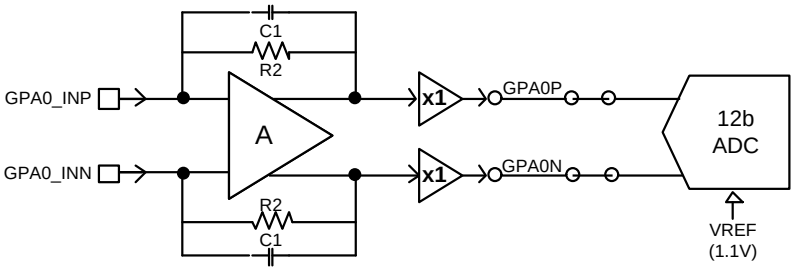


Figure 5-16 Block Diagram of TIA Configuration in GP Analog0

Table 5-5 describes the detail configurations for the gain and bandwidth of TIA in GP Analog0.

Table 5-5 Gain and Bandwidth of TIA in GP Analog0

GPA0_R2_300K	GAP0_R2_CTRL[1:0]	GPA0_C1_CTRL[1:0]	Gain [MΩ]	–3 dB BW [kHz]
0	00	00	1.30	16.29
		01		12.22
		10		9.77
		11		8.14
	01	00	2.60	8.14
		01		6.11
		10		4.89
		11		4.07
	10	00	5.21	4.07
		01		3.05
		10		2.44
		11		2.04
	11	00	10.42	2.04
		01		1.53
		10		1.22
		11		1.02
1	XX	00	0.60	35.29
		01		26.47
		10		21.17
		11		17.65

5.2.4.1.1.2 VGA in GP Analog0

For VGA configuration illustrated in *Figure 5-17*, GPA0_INP/INN can receive differential voltage signal (for example, from bridge circuit). The VGA provides pseudo-differential voltage gain of 1+R2/R1. This gain can be adjusted in four steps according to the register value of GPA0_R1_CTRL[1:0]. Note that the value of R2 for VGA is cannot be adjusted. Similar to TIA, C1 in parallel with R2 provides first-order anti-alias filter for the ADC. The value of C1 can be configured in four steps according to the register value of GPA0_C1_CTRL[1:0]. Note that the common-mode voltage to GPA0_INP/INN must be 0.55 V as the VGA behaves as a non-inverting amplifier and internally biased. Use the following equations to determine the gain and bandwidth of VGA.

$$\textbf{Gain}\ (\mathbf{V/V}) = 1 + \frac{R_2}{R_1}$$

$$\textbf{Bandwidth}\ (\mathbf{Hz}) = \frac{1}{2 \cdot \pi \cdot R_2 \cdot C_1}$$

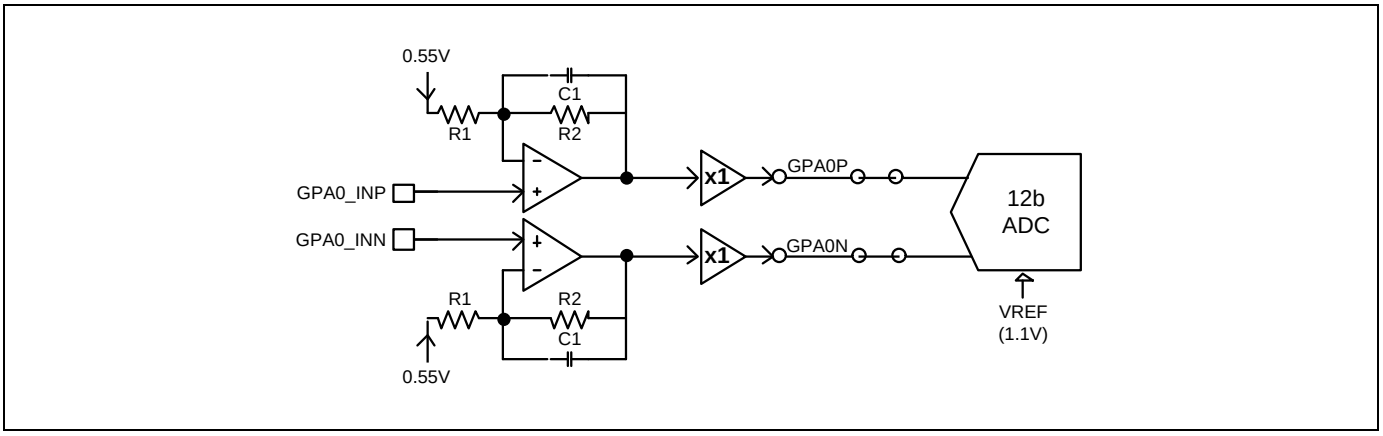


Figure 5-17 Block Diagram of VGA Configuration in GP Analog0

Table 5-6 describes the detail configurations for the gain and bandwidth of VGA in GP Analog0.

Table 5-6 Gain and Bandwidth of VGA in GP Analog0

GPA0_R2_CTRL[1:0]	GAP0_R1_CTRL[1:0]	Gain [V/V]
11	00	15.84
	01	7.94
	10	3.98
	11	1.99

GPA0_R2_CTRL[1:0]	GAP0_C1_CTRL[1:0]	BW [kHz]
11	00	2.04
	01	1.53
	10	1.22
	11	1.02

5.2.4.1.1.3 LPF in GP Analog0

For LPF configuration illustrated in *Figure 5-18*, R2 and C1 provide passive LPF prior to ADC. In this configuration, all amplifiers are turned off for low-power consumption. Unlike VGA, the common-mode voltage inputs at GPA0_INP/INN are not limited to 0.55 V. Depending on the register value of R2 and C1, the –3 dB bandwidth is configured in wide range from 1 kHz to 16.3 kHz. Use the following equations to determine the bandwidth of LPF.

$$\textbf{Bandwidth}\ (\textbf{Hz}) = \frac{1}{2 \cdot \pi \cdot R_2 \cdot C_1}$$

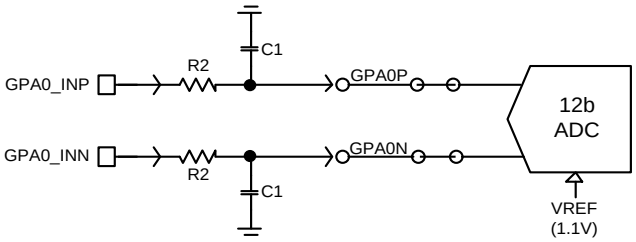


Figure 5-18 Block Diagram of LPF Configuration in GP Analog0

Table 5-7 describes the detail configurations for bandwidth of LPF in GP Analog0.

Table 5-7 Bandwidth of LPF in GP Analog0

GPA0_R2_CTRL[1:0]	GAP0_C1_CTRL[1:0]	BW [kHz]
00	00	16.29
	01	12.22
	10	9.77
	11	8.14
01	00	8.14
	01	6.11
	10	4.89
	11	4.07
10	00	4.07
	01	3.05
	10	2.44
	11	2.04
11	00	2.04
	01	1.53
	10	1.22
	11	1.02

5.2.4.1.2 Switch Configurations for GP Analog1

GP Analog1 integrates nine switches which can be configured by the register value of GPA1_SW_SEL[8:0]. *Table 5-8* describes the detail switch configurations.

Table 5-8 Switch Configurations in GP Analog1

Stage	Interface	GPA1_SW_SEL[8:0]								
		8	7	6	5	4	3	2	1	0
1st stage	Attenuator	0	–	–	0	1	0	1	1	0
	Die temperature	0	–	–	1	1	0	0	0	0
	Bypass (1st-stage)	0	–	–	0	1	0	0	1	0
	GP Switch	0	–	–	0	1	0	0	0	1
2nd stage	ADC driver	0	1	0	–	–	–	–	–	–
	Bypass (2nd-stage)	0	0	1	–	–	–	–	–	–

5.2.4.1.2.1 Voltage Attenuator in GP Analog1

GP Analog1 integrates 100 kΩ internal resistor, Rint, at inputs (between GPA1_INP and GPA1_INN). With the help of external resistor in series, Rext illustrated in *Figure 5-19*, it can behave as a voltage attenuator. Use the following equation to determine the voltage attenuation configuration in GP analog1.

$$\textbf{Attenuation}\ (\mathbf{V/V}) = \frac{\mathbf{Rint}}{\mathbf{2 \cdot Rext + Rint}}$$

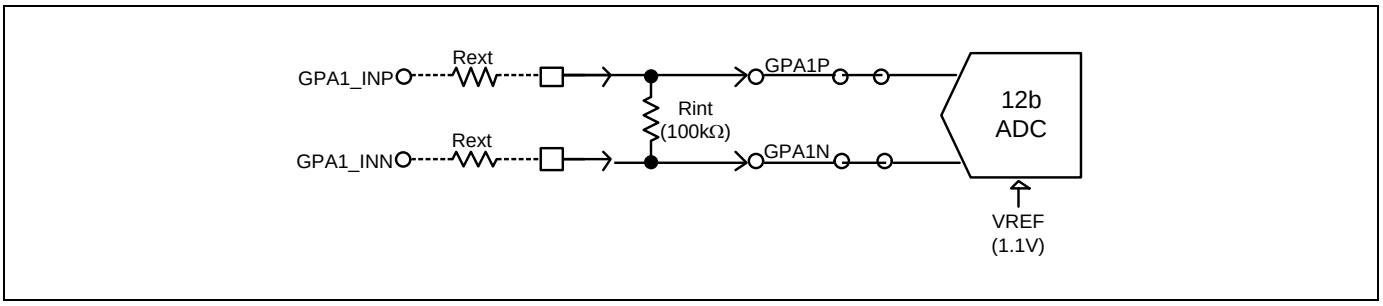


Figure 5-19 Block Diagram of Voltage Attenuator Configuration in GP Analog1

5.2.4.1.2.2 Die Temperature Sensor in GP Analog1

GP Analog1 integrates thermal diodes as illustrated in *Figure 5-20*. The ADC can measure voltage difference of diode junctions with respect to temperature. Use the following equation to determine the voltage difference of diode junctions and ADC code.

$$\mathbf{V1 - V2\ \ (V)\ \ = \frac{kT}{q} \times ln27}$$

$$\mathbf{ADC\ \ code\ \ = 2048 + \frac{V1 - V2}{1LSB}}$$

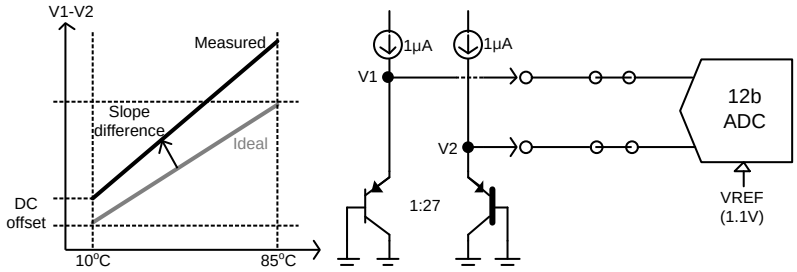


Figure 5-20 Block Diagram of Die Temperature Sensor Configuration in GP Analog1

Practically, there exists slope difference and DC offset between measured transfer curve and an ideal transfer curve.

To compensate this, V1 and V2 are measured at temperature of 10 °C and 85 °C, respectively. The measured 12 bit ADC code is then compensated (DC offset and slope difference) by the digital signal processing (Software). The following equation is considered for the transfer curve compensation to determine the calibrated temperature value of Tsense.

$$\mathbf{Tcalib\ \ = (Tsense - TE1) \times \frac{D85 - D10}{TE2 - TE1} + TE1 - (TE1 - D10)}$$

Where Tsense is the practically measured ADC code including DC offset and slope error. Tcalib is the calibrated ADC code of Tsense, TE1 corresponds to the measured ADC code at 10 °C, and TE2 corresponds to the measured ADC code at 85 °C. D85 is the ideal ADC code(=2237) at 85 °C, and D10 is the ideal ADC code(=2198) at 10 °C. According to the above equation, the last term (TE1- D10) represents DC offset and the remaining term represents the slope compensation.

5.2.4.1.2.3 Analog Switch in GP Analog1

GP Analog1 provides single analog switch illustrated in *Figure 5-21* which can be programmed by register value of GPA1_SW_SEL[0]. GPA1_INP and GPA1_INN are used as switch terminals. Note that other circuits such as temperature sensor and ADC are completely isolated from GPA1_INP/INN in this configuration.

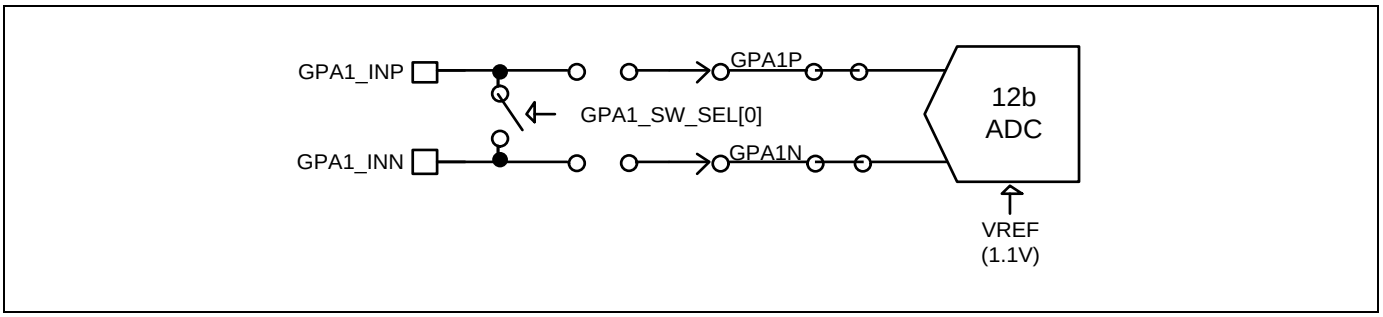


Figure 5-21 Block Diagram of Analog Switch in GP Analog1

5.2.4.2 Register Description

This section describes the register map information and its associated registers.

5.2.4.2.1 Register Map Summary

- Base Address: 0x4001_A000

Register	Offset	Description	Reset Value
AFE_CLK_CTRL	0x0000	AFE_CLK_CTRL	0x0000_00FF
AFE_RST_CTRL	0x0004	AFE_RST_CTRL	0x0000_000F
GP_ADC0	0x0014	GP Analog0 Setting	0x0A00_0000
GP_ADC1	0x0018	GP Analog1 Setting	0x0000_0920
REGULATOR_CTRL0	0x0020	REGULATOR_CTRL0	0x0018_1818
REGULATOR_CTRL1	0x0024	REGULATOR_CTRL1	0x0000_8818
TMPX	0x0038	Test MUX Control	0x0000_0000
SAR_ADC_CON	0x0644	SAR ADC OSR mode selections	0x0000_0000
SAR_ADC_CTRL	0x0648	SAR ADC enable controls	0x0008_3330
SDADC_CTRL1	0x0700	GP24 ADC Control 1	0x0000_0004
SDADC_CTRL2	0x0704	GP24 ADC Control 2	0x0000_0004
SDADC_CTRL3	0x0708	GP24 ADC Control 3	0x0000_0007
GPADC_LDO_CTRL	0x0714	GP24 ADC_LDO_control	0x0000_0000

NOTE: If reserved or empty addresses in the register map are changed, S1SBP6A cannot guarantee normal operation.

5.2.4.2.1.1 AFE_CLK_CTRL

- Base Address: 0x4001_A000
- Address = Base Address + 0x0000, Reset Value = 0x0000_00FF

Name	Bit	Type	Description	Reset Value
SEL_SAMPLE_CLK	[8]	RW	* Sample clock select 1: Select 16 kHz sample clock with 32 kHz sample source clock 0: Select 2 kHz sample clock with 32 kHz sample source clock	0x0000_0000
SAR_ADC2_EN	[7]	RW	* SAR ADC2 clock enable 1: Clock enabled. 0: Clock gated.	0x0000_0001
SAR_ADC1_EN	[6]	RW	* SAR ADC1 clock enable 1: Clock enabled. 0: Clock gated.	0x0000_0001
SAR_ADC0_EN	[5]	RW	* SAR ADC0 clock enable 1: Clock enabled. 0: Clock gated.	0x0000_0001
GSR_CK_EN	[4]	RW	* GSR clock enable 1: Clock enabled. 0: Clock gated.	0x0000_0001
RSVD1	[3]	RW	Reserved.	0x0000_0001
PPG_CK_EN	[2]	RW	* PPG clock enable 1: Clock enabled. 0: Clock gated.	0x0000_0001
BIA_CK_EN	[1]	RW	* BIA clock enable 1: Clock enabled. 0: Clock gated.	0x0000_0001
ECG_CK_EN	[0]	RW	* ECG clock enable 1: Clock enabled. 0: Clock gated.	0x0000_0001

5.2.4.2.1.2 AFE_RST_CTRL

- Base Address: 0x4001_A000
- Address = Base Address + 0x0004, Reset Value = 0x0000_000F

Name	Bit	Type	Description	Reset Value
GSR_RESETB	[3]	RW	* GSR Logic Software Reset 1: Release reset 0: Assert reset	0x0000_0001
BIA_RESETB	[2]	RW	* BIA Logic Software Reset 1: Release reset 0: Assert reset	0x0000_0001
PPG_RESETB	[1]	RW	* PPG Logic Software Reset 1: Release reset 0: Assert reset	0x0000_0001
ECG_RESETB	[0]	RW	* ECG Logic Software Reset 1: Release reset 0: Assert reset	0x0000_0001

5.2.4.2.1.3 GP_ADC0

- Base Address: 0x4001_A000
- Address = Base Address + 0x0014, Reset Value = 0x0A00_0000

Name	Bit	Type	Description	Reset Value
SW_SEL	[27:16]	RW	Switch selection for GP Analog0. For more information, refer to *Table 5-4*.	0x0000_0A00
RSVD0	[15:14]	RW	Reserved	0x0000_0000
C1_CTRL	[13:12]	RW	Capacitor control signals for GP Analog0 TIA, VGA, and LPF. For more information, refer to *Table 5-5*, *Table 5-6*, and *Table 5-7*.	0x0000_0000
RSVD1	[11:9]	RW	Reserved	0x0000_0000
R2_300K	[8]	RW	Resistor control signal for GP Analog0 TIA. For more information, refer to *Table 5-5*.	0x0000_0000
R2_CTRL	[7:6]	RW	Resistor control signals for GP Analog0 TIA, VGA, and LPF. For more information, refer to *Table 5-5*, *Table 5-6*, and *Table 5-7*.	0x0000_0000
R1_CTRL	[5:4]	RW	Resistor control signals for GP Analog0 VGA. For more information, refer to *Table 5-6*.	0x0000_0000
RSVD2	[3:2]	RW	Reserved	0x0000_0000
AMP1_EN	[1]	RW	2nd stage ADC driver for GP Analog0 enable signal. 1: enable, 0: disable	0x0000_0000
AMP0_EN	[0]	RW	1st stage amplifier for GP Analog0 TIA, VGA enable signal. 1: enable, 0: disable	0x0000_0000

5.2.4.2.1.4 GP_ADC1

- Base Address: 0x4001_A000
- Address = Base Address + 0x0018, Reset Value = 0x0000_0920

Name	Bit	Type	Description	Reset Value
SW_SEL	[12:4]	RW	Switch selection for GP Analog1. For more information, refer to *Table 5-8*.	0x0000_0092
ENABLE	[0]	RW	2nd stage ADC driver for GP Analog1 enable signal. 1: Enable, 0: Disable	0x0000_0000

5.2.4.2.1.5 REGULATOR_CTRL0

- Base Address: 0x4001_A000
- Address = Base Address + 0x0020, Reset Value = 0x0018_1818

Name	Bit	Type	Description	Reset Value
CLDO_VCTRL	[20:16]	RW	LDO3 output voltage 00000 : 0.5 V, 11111 : 1.275 V, step=25 mV	0x0000_0018
RSVD0	[15:13]	RW	Reserved	0x0000_0000
PLDO_VCTRL	[12:8]	RW	LDO2 output voltage 00000 : 0.5 V, 11111 : 1.275 V, step=25 mV	0x0000_0018
RSVD1	[7:5]	RW	Reserved	0x0000_0000
ALDO_VCTRL	[4:0]	RW	LDO1 output voltage 00000 : 0.5 V, 11111 : 1.275 V, step=25 mV	0x0000_0018

5.2.4.2.1.6 REGULATOR_CTRL1

- Base Address: 0x4001_A000
- Address = Base Address + 0x0024, Reset Value = 0x0000_8818

Name	Bit	Type	Description	Reset Value
PBOR_RBTRIM	[15:12]	RW	Reference voltage trimming (default 0.475 V,0.365 V)	0x0000_0008
V0P8_RBTRIM	[11:8]	RW	Reference voltage trimming (default 0.475 V,0.365 V)	0x0000_0008
RSVD0	[7:5]	RW	Reserved	0x0000_0000
MLDO_VCTRL	[4:0]	RW	LDO4 output voltage 00000 : 0.5 V, 11111 : 1.275 V, step = 25 mV	0x0000_0018

5.2.4.2.1.7 TMPX

- Base Address: 0x4001_A000
- Address = Base Address + 0x0038, Reset Value = 0x0000_0000, Default Value for GSR=0x0000_0553

Name	Bit	Type	Description	Reset Value
SELN	[11:8]	RW	Negative TMPX MUX selection signal. 0000: External input voltage(TAIN), 0101: GSR_NOUT	0x0000_0000
SELP	[7:4]	RW	Positive TMPX MUX selection signal. 0000: External input voltage(TAIP), 0101: GSR_POUT	0x0000_0000
BUFN_BYPASS	[3]	RW	Negative TMPX output buffer bypass signal. 1:bBpass, 0:Pass	0x0000_0000
BUFP_BYPASS	[2]	RW	Positive TMPX output buffer bypass signal. 1:Bypass, 0:Pass	0x0000_0000
ENN	[1]	RW	Negative TMPX output buffer enable signal. 1:Enable, 0:Disable	0x0000_0000
ENP	[0]	RW	Positive TMPX output buffer enable signal. 1:Enable, 0:Disable	0x0000_0000

5.2.4.2.1.8 SAR_ADC_CON

- Base Address: 0x4001_A000
- Address = Base Address + 0x0644, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
OSR_MODE2	[10:8]	RW	3'b0 : OSR0 (no decimation) 3'b1 : OSR1 (2 sample decimation) 3'b2 : OSR2 (4 sample decimation) 3'b3 : OSR3 (8 sample decimation) 3'b4 : OSR4 (16sample decimation)	0x0000_0000
OSR_MODE1	[6:4]	RW	3'b0 : OSR0 (no decimation) 3'b1 : OSR1 (2 sample decimation) 3'b2 : OSR2 (4 sample decimation) 3'b3 : OSR3 (8 sample decimation) 3'b4 : OSR4 (16sample decimation)	0x0000_0000
OSR_MODE0	[2:0]	RW	3'b0 : OSR0(no decimation) 3'b1 : OSR1(2 sample decimation) 3'b2 : OSR2(4 sample decimation) 3'b3 : OSR3(8 sample decimation) 3'b4 : OSR4(16sample decimation)	0x0000_0000

5.2.4.2.1.9 SAR_ADC_CTRL

- Base Address: 0x4001_A000
- Address = Base Address + 0x0648, Reset Value = 0x0008_3330

Name	Bit	Type	Description	Reset Value
ENADC	[3:1]	RW	Enable signal for each ADC. 100: Enable SAR2, 010: Enable SAR1, 001: Enable SAR0	0x0000_0000
EN	[0]	RW	Enable signal for All 3 SAR ADCs. 1: Enable, 0: Disable	0x0000_0000

5.2.4.2.1.10 SDADC_CTRL1

- Base Address: 0x4001_A000
- Address = Base Address + 0x0700, Reset Value = 0x0000_0004

Name	Bit	Type	Description	Reset Value
SDADC_RESET	[7]	RW	SD modulator and control logic reset 0: Release reset 1: Assert reset	0x0000_0000
SDADC_EN_BUF	[6]	RW	SD BUF enable signal. 1: Enable, 0: Disable	0x0000_0000
SDADC_EN	[5]	RW	SD ADC enable signal. 1: Enable, 0: Disable	0x0000_0000
SDADC_START	[4]	RW	SD control logic start. 64kHz clock is enabled by the register	0x0000_0000
SDADC_DFILTER	[3:2]	RW	Data rate selection for digital filter 0: 1 kHz 1: 500 Hz 2: 250 Hz 3: 125 Hz	0x0000_0001
SDADC_SEL_INPUT	[1:0]	RW	SD Input MUX control signal. 0: Differential input1(VIP<0>,VIN<0>) 1: Single-ended input(VIP<1>) 2: INL test 3: INL test	0x0000_0000

5.2.4.2.1.11 SDADC_CTRL2

- Base Address: 0x4001_A000
- Address = Base Address + 0x0704, Reset Value = 0x0000_0004

Name	Bit	Type	Description	Reset Value
SDADC_SEL_VCM	[2:0]	RW	SD VCM level control 0: 0.31 V 1: 0.55 V 2: 0.78 V 3: 1.02 V 4: 1.25 V 5: 1.48 V 6: 1.72 V 7: 1.95 V	0x0000_0004

5.2.4.2.1.12 SDADC_CTRL3

- Base Address: 0x4001_A000
- Address = Base Address + 0x0708, Reset Value = 0x0000_0007

Name	Bit	Type	Description	Reset Value
SDADC_BUF_BYPASS	[3]	RW	SD BUF bypass-ability. 1: Bypass, 0: Pass	0x0000_0000
SDADC_EN_DEM	[2]	RW	SD DEM enable signal. 1: Enable, 0: Disable	0x0000_0001
SDADC_EN_CHOP_BUF	[1]	RW	SD BUF chopping clock disability. 1: Enable chopping, 0: Disable chopping	0x0000_0001
SDADC_EN_CHOP_DSM	[0]	RW	SD DSM chopping clock disability. 1: Enable chopping, 0: Disable chopping	0x0000_0001

5.2.4.2.1.13 GPADC_LDO_CTRL

- Base Address: 0x4001_A000
- Address = Base Address + 0x0714, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
SDADC_LDO_EN	[0]	RW	SD LDO enable signal. 1: Enable, 0: Disable	0x0000_0000

5.2.5 FIFO Control

5.2.5.1 Overview

The AFE control logic has the following four functions:

- SAR-ADC channel separation/decimation
- Six 16-bit FIFOs and three 24-bit FIFO
- DMA controller of FIFO
- Special function registers for AFE controller

5.2.5.2 Feature

AFE Controller has nine FIFOs, six FIFOs for 12 bits SAR-ADCs, one FIFO for 24 bits Sigma-Delta ADC, and two FIFOs for 24 bits Incremental ADC. Each FIFO has 16 depths. All FIFOs operate in PCLK domain. Each FIFO has three interrupt sources which are FULL, EMPTY, and READY. Only one combined interrupt signal is generated from FIFOs and it can be cleared by writing 1 to INTR_CLR register. Interrupt masking is available using FIFO_INTR_MASK registers. Ready interrupt is generated when the number of data saved in FIFO is larger than the number of data set by FIFO_READY_SIZE_SET register. Register control also supports software reset of FIFO. DMA controller in FIFO generates DMA request signals according to the register setting. Use FIFO_READ_DATA_SIZE_SET register to set the number of data which generates the DMA signal. After the controller gets acknowledge signal from µDMA, the request signals are automatically cleared. *Figure 5-22* illustrates the block diagram of AFE FIFO controller.

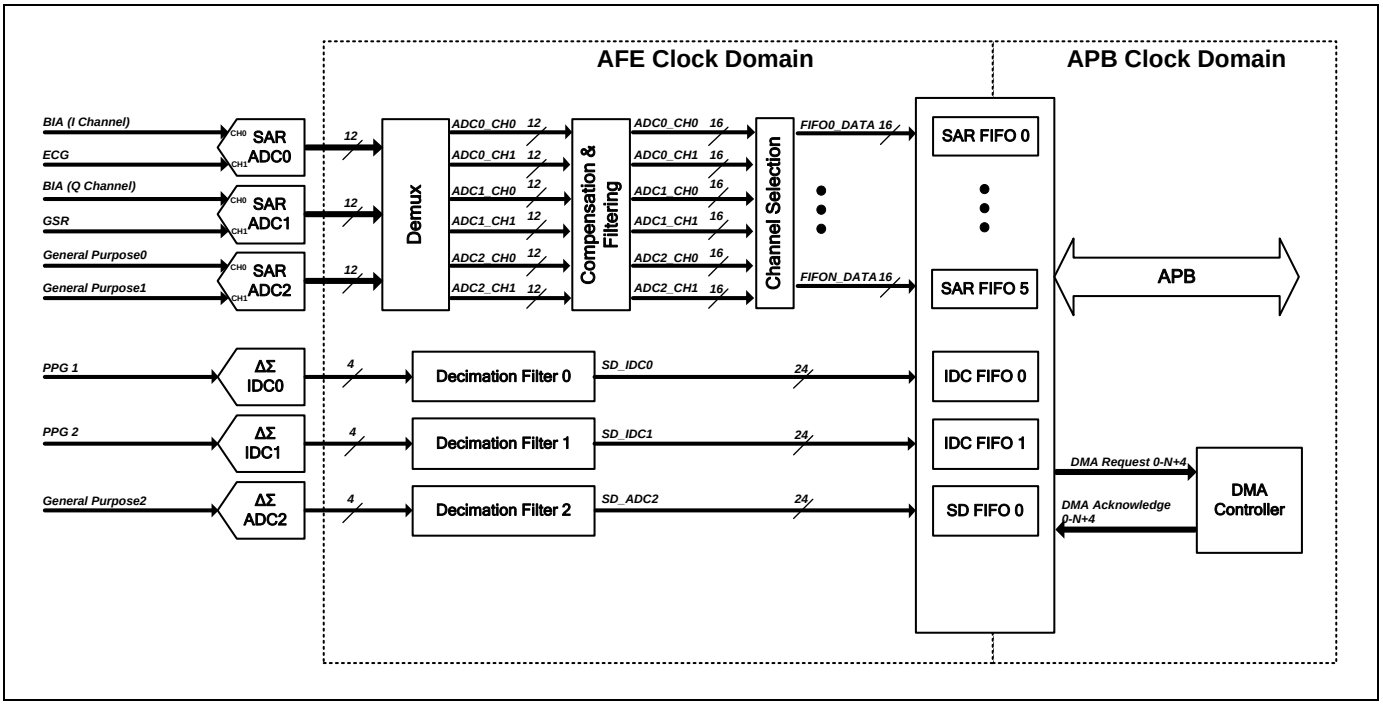


Figure 5-22 Block Diagram of AFE FIFO Controller

5.2.5.3 Register Description

This section describes the register map information and its associated registers.

5.2.5.3.1 Register Map Summary

- Base Address: 0x4001_A000

Register	Offset	Description	Reset Value
FIFO_INTR_MASK	0x0500	FIFO_INTR_MASK	0x0249_2492
FIFO_SW_RESET	0x0504	FIFO_SW_RESET	0x0000_0000
FIFO_DMA_SIZE0	0x0508	FIFO_DMA_SIZE0	0x0000_0000
FIFO_READY_SIZE0	0x050C	FIFO_READY_SIZE0	0x0000_0000
FIFO_ENABLE	0x0510	FIFO_ENABLE	0x0000_0000
FIFO_DMA_ENABLE	0x0514	FIFO_DMA_ENABLE	0x0000_003F
FIFO_INT_CLEAR	0x0518	FIFO_INT_CLEAR	0x0000_0000
FIFO0_READ_DATA	0x051C	FIFO0_READ_DATA	0x0000_0000
FIFO1_READ_DATA	0x0520	FIFO1_READ_DATA	0x0000_0000
FIFO2_READ_DATA	0x0524	FIFO2_READ_DATA	0x0000_0000
FIFO3_READ_DATA	0x0528	FIFO3_READ_DATA	0x0000_0000
FIFO4_READ_DATA	0x052C	FIFO4_READ_DATA	0x0000_0000
FIFO5_READ_DATA	0x0530	FIFO5_READ_DATA	0x0000_0000
FIFO6_READ_DATA	0x0534	FIFO6_READ_DATA	0x0000_0000
FIFO7_READ_DATA	0x0538	FIFO7_READ_DATA	0x0000_0000
FIFO8_READ_DATA	0x053C	FIFO8_READ_DATA	0x0000_0000
FIFO_DATA_SAR	0x0544	FIFO_DATA_SAR	0x0000_0000
FIFO_DATA_IDC	0x0548	FIFO_DATA_IDC	0x0000_0000
FIFO_STATUS	0x054C	FIFO_STATUS	0x0249_2492
FIFO_RCLK_MANUAL_CG_EN	0x0550	FIFO_RCLK_MANUAL_CG_EN	0x0000_0000
FIFO_RCLK_MANUAL_CG	0x0554	FIFO_RCLK_MANUAL_CG	0x0000_0000
FIFO_DMA_SIZE1	0x0558	FIFO_DMA_SIZE1	0x0000_0000
FIFO_READY_SIZE1	0x055C	FIFO_READY_SIZE1	0x0000_0000
FIFO_DATA_SDC	0x0560	FIFO_DATA_SDC	0x0000_0000
FIFO_INT_STATUS	0x0564	FIFO_INT_STATUS	0x0000_0000
SAR_SEL	0x0600	SAR_SEL	0x0002_C688
DC_COMPEN_ADC0	0x0604	DC_COMPEN_ADC0	0x0000_0000
DC_COMPEN_ADC1	0x0608	DC_COMPEN_ADC1	0x0000_0000
DC_COMPEN_ADC2	0x060C	DC_COMPEN_ADC2	0x0000_0000

Register	Offset	Description	Reset Value
SAR_ADC0_CH0_DATA	0x061C	SAR_ADC0_CH0_DATA	0x0000_0000
SAR_ADC0_CH1_DATA	0x0620	SAR_ADC0_CH1_DATA	0x0000_0000
SAR_ADC1_CH0_DATA	0x0624	SAR_ADC1_CH0_DATA	0x0000_0000
SAR_ADC1_CH1_DATA	0x0628	SAR_ADC1_CH1_DATA	0x0000_0000
SAR_ADC2_CH0_DATA	0x062C	SAR_ADC2_CH0_DATA	0x0000_0000
SAR_ADC2_CH1_DATA	0x0630	SAR_ADC2_CH1_DATA	0x0000_0000
SD_ADC0_DATA	0x0634	SD_ADC0_DATA	0x0000_0000
SD_ADC1_DATA	0x0638	SD_ADC1_DATA	0x0000_0000
SD_ADC2_DATA	0x063C	SD_ADC2_DATA	0x0000_0000

NOTE: If reserved or empty addresses in the register map are changed, S1SBP6A cannot guarantee normal operation.

5.2.5.3.1.1 FIFO_INTR_MASK

- Base Address: 0x4001_A000
- Address = Base Address + 0x0500, Reset Value = 0x0249_2492

Name	Bit	Type	Description	Reset Value
FULL8	[26]	RW	* FIFO8 Full Interrupt	0x0000_0000
EMPTY8	[25]	RW	* FIFO8 Empty Interrupt	0x0000_0001
READY8	[24]	RW	* FIFO8 Ready Interrupt	0x0000_0000
FULL7	[23]	RW	* FIFO7 Full Interrupt	0x0000_0000
EMPTY7	[22]	RW	* FIFO7 Empty Interrupt	0x0000_0001
READY7	[21]	RW	* FIFO7 Ready Interrupt	0x0000_0000
FULL6	[20]	RW	* FIFO6 Full Interrupt	0x0000_0000
EMPTY6	[19]	RW	* FIFO6 Empty Interrupt	0x0000_0001
READY6	[18]	RW	* FIFO6 Ready Interrupt	0x0000_0000
FULL5	[17]	RW	* FIFO5 Full Interrupt	0x0000_0000
EMPTY5	[16]	RW	* FIFO5 Empty Interrupt	0x0000_0001
READY5	[15]	RW	* FIFO5 Ready Interrupt	0x0000_0000
FULL4	[14]	RW	* FIFO4 Full Interrupt	0x0000_0000
EMPTY4	[13]	RW	* FIFO4 Empty Interrupt	0x0000_0001
READY4	[12]	RW	* FIFO4 Ready Interrupt	0x0000_0000
FULL3	[11]	RW	* FIFO3 Full Interrupt	0x0000_0000
EMPTY3	[10]	RW	* FIFO3 Empty Interrupt	0x0000_0001
READY3	[9]	RW	* FIFO3 Ready Interrupt	0x0000_0000
FULL2	[8]	RW	* FIFO2 Full Interrupt	0x0000_0000
EMPTY2	[7]	RW	* FIFO2 Empty Interrupt	0x0000_0001
READY2	[6]	RW	* FIFO2 Ready Interrupt	0x0000_0000
FULL1	[5]	RW	* FIFO1 Full Interrupt	0x0000_0000
EMPTY1	[4]	RW	* FIFO1 Empty Interrupt	0x0000_0001
READY1	[3]	RW	* FIFO1 Ready Interrupt	0x0000_0000
FULL0	[2]	RW	* FIFO0 Full Interrupt	0x0000_0000
EMPTY0	[1]	RW	* FIFO0 Empty Interrupt	0x0000_0001
READY0	[0]	RW	* FIFO0 Ready Interrupt	0x0000_0000

5.2.5.3.1.2 FIFO_SW_RESET

- Base Address: 0x4001_A000
- Address = Base Address + 0x0504, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
FIFO_SW_RESET	[8:0]	RW	FIFO reset([0]:FIFO0 ~ [8]:FIFO8) 1'b1 : FIFO Reset enable 1'b0 : FIFO Reset disable	0x0000_0000

5.2.5.3.1.3 FIFO_DMA_SIZE0

- Base Address: 0x4001_A000
- Address = Base Address + 0x0508, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
SET5	[23:20]	RW	* Select the number of data stored in FIFO5 to generate a DMA request. - The number of data which generates a DMA request is (DMA_SIZE5+1).	0x0000_0000
SET4	[19:16]	RW	* Select the number of data stored in FIFO4 to generate a DMA request. - The number of data which generates a DMA request is (DMA_SIZE4+1).	0x0000_0000
SET3	[15:12]	RW	* Select the number of data stored in FIFO3 to generate a DMA request. - The number of data which generates a DMA request is (DMA_SIZE3+1).	0x0000_0000
SET2	[11:8]	RW	* Select the number of data stored in FIFO2 to generate a DMA request. - The number of data which generates a DMA request is (DMA_SIZE2+1).	0x0000_0000
SET1	[7:4]	RW	* Select the number of data stored in FIFO1 to generate a DMA request. - The number of data which generates a DMA request is (DMA_SIZE1+1).	0x0000_0000
SET0	[3:0]	RW	* Select the number of data stored in FIFO0 to generate a DMA request. - The number of data which generates a DMA request is (DMA_SIZE0+1).	0x0000_0000

5.2.5.3.1.4 FIFO_READY_SIZE0

- Base Address: 0x4001_A000
- Address = Base Address + 0x050C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
SET5	[23:20]	RW	* Select the number of data stored in FIFO5 to generate the FIFO_READY5 interrupt. - The number of data which generates FIFO_READY5 interrupt is (FIFO_READY_SIZE5+1).	0x0000_0000
SET4	[19:16]	RW	* Select the number of data stored in FIFO4 to generate the FIFO_READY4 interrupt. - The number of data which generates FIFO_READY4 interrupt is (FIFO_READY_SIZE4+1).	0x0000_0000
SET3	[15:12]	RW	* Select the number of data stored in FIFO3 to generate the FIFO_READY3 interrupt. - The number of data which generates FIFO_READY3 interrupt is (FIFO_READY_SIZE3+1).	0x0000_0000
SET2	[11:8]	RW	* Select the number of data stored in FIFO2 to generate the FIFO_READY2 interrupt. - The number of data which generates FIFO_READY2 interrupt is (FIFO_READY_SIZE2+1).	0x0000_0000
SET1	[7:4]	RW	* Select the number of data stored in FIFO1 to generate the FIFO_READY1 interrupt. - The number of data which generates FIFO_READY1 interrupt is (FIFO_READY_SIZE1+1).	0x0000_0000
SET0	[3:0]	RW	* Select the number of data stored in FIFO0 to generate the FIFO_READY0 interrupt. - The number of data which generates FIFO_READY0 interrupt is (FIFO_READY_SIZE0+1).	0x0000_0000

5.2.5.3.1.5 FIFO_ENABLE

- Base Address: 0x4001_A000
- Address = Base Address + 0x0510, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
FIFO_ENABLE	[8:0]	RW	FIFO Block enable([0]:FIFO0 ~ [8]:FIFO8) 1'b1 : FIFO Block enable 1'b0 : FIFO Block disable	0x0000_0000

5.2.5.3.1.6 FIFO_DMA_ENABLE

- Base Address: 0x4001_A000
- Address = Base Address + 0x0514, Reset Value = 0x0000_003F

Name	Bit	Type	Description	Reset Value
FIFO_DMA_ENABLE	[8:0]	RW	FIFO DMA Interface enable([0]:FIFO0 ~ [8]:FIFO8) 1'b1 : Enable 1'b0 : Disable	0x0000_003F

5.2.5.3.1.7 FIFO_INT_CLEAR

- Base Address: 0x4001_A000
- Address = Base Address + 0x0518, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
FIFO_INT_CLEAR	[0]	RW	FIFO Interrupt clear 1'b1 : Clear enable 1'b0 : Clear disable	0x0000_0000

5.2.5.3.1.8 FIFO0_READ_DATA

- Base Address: 0x4001_A000
- Address = Base Address + 0x051C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
FIFO0_READ_DATA	[15:0]	RW	FIFO0_READ_DATA	0x0000_0000

5.2.5.3.1.9 FIFO1_READ_DATA

- Base Address: 0x4001_A000
- Address = Base Address + 0x0520, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
FIFO1_READ_DATA	[15:0]	RW	FIFO1_READ_DATA	0x0000_0000

5.2.5.3.1.10 FIFO2_READ_DATA

- Base Address: 0x4001_A000
- Address = Base Address + 0x0524, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
FIFO2_READ_DATA	[15:0]	RW	FIFO2_READ_DATA	0x0000_0000

5.2.5.3.1.11 FIFO3_READ_DATA

- Base Address: 0x4001_A000
- Address = Base Address + 0x0528, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
FIFO3_READ_DATA	[15:0]	RW	FIFO3_READ_DATA	0x0000_0000

5.2.5.3.1.12 FIFO4_READ_DATA

- Base Address: 0x4001_A000
- Address = Base Address + 0x052C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
FIFO4_READ_DATA	[15:0]	RW	FIFO4_READ_DATA	0x0000_0000

5.2.5.3.1.13 FIFO5_READ_DATA

- Base Address: 0x4001_A000
- Address = Base Address + 0x0530, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
FIFO5_READ_DATA	[15:0]	RW	FIFO5_READ_DATA	0x0000_0000

5.2.5.3.1.14 FIFO6_READ_DATA

- Base Address: 0x4001_A000
- Address = Base Address + 0x0534, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
FIFO6_READ_DATA	[25:0]	RW	FIFO6_READ_DATA	0x0000_0000

5.2.5.3.1.15 FIFO7_READ_DATA

- Base Address: 0x4001_A000
- Address = Base Address + 0x0538, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
FIFO7_READ_DATA	[25:0]	RW	FIFO7_READ_DATA	0x0000_0000

5.2.5.3.1.16 FIFO8_READ_DATA

- Base Address: 0x4001_A000
- Address = Base Address + 0x053C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
FIFO8_READ_DATA	[23:0]	RW	FIFO8_READ_DATA	0x0000_0000

5.2.5.3.1.17 FIFO_DATA_SAR

- Base Address: 0x4001_A000
- Address = Base Address + 0x0544, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
FIFO_DATA_SAR	[29:0]	R	SAR FIFO Read data	0x0000_0000

5.2.5.3.1.18 FIFO_DATA_IDC

- Base Address: 0x4001_A000
- Address = Base Address + 0x0548, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
FIFO_DATA_IDC	[13:0]	R	IDC FIFO Read data	0x0000_0000

5.2.5.3.1.19 FIFO_STATUS

- Base Address: 0x4001_A000
- Address = Base Address + 0x054C, Reset Value = 0x0249_2492

Name	Bit	Type	Description	Reset Value
FIFO_STATUS	[26:0]	R	FIFO_STATUS_READ	0x0249_2492

5.2.5.3.1.20 FIFO_RCLK_MANUAL_CG_EN

- Base Address: 0x4001_A000
- Address = Base Address + 0x0550, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
FIFO_RCLK_MANUAL_CG_EN	[8:0]	RW	FIFO read clock gating enable ([0]:FIFO0 ~ [8]:FIFO8) 1'b1 : Enable 1'b0 : Disable	0x0000_0000

5.2.5.3.1.21 FIFO_RCLK_MANUAL_CG

- Base Address: 0x4001_A000
- Address = Base Address + 0x0554, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
FIFO_RCLK_MANUAL_CG	[8:0]	RW	FIFO read clock gating ([0]:FIFO0 ~ [8]:FIFO8) 1'b1 : Clock disable 1'b0 : Clock enable	0x0000_0000

5.2.5.3.1.22 FIFO_DMA_SIZE1

- Base Address: 0x4001_A000
- Address = Base Address + 0x0558, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
SET8	[19:16]	RW	* Select the number of data stored in FIFO8 to generate a DMA request. - The number of data which generates a DMA request is (DMA_SIZE8+1).	0x0000_0000
RSVD0	[15:14]	RW	Reserved	0x0000_0000
SET7	[13:8]	RW	* Select the number of data stored in FIFO7 to generate a DMA request. - The number of data which generates a DMA request is (DMA_SIZE7+1).	0x0000_0000
RSVD1	[7:6]	RW	Reserved	0x0000_0000
SET6	[5:0]	RW	* Select the number of data stored in FIFO6 to generate a DMA request. - The number of data which generates a DMA request is (DMA_SIZE6+1).	0x0000_0000

5.2.5.3.1.23 FIFO_READY_SIZE1

- Base Address: 0x4001_A000
- Address = Base Address + 0x055C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
SET8	[19:16]	RW	* Select the number of data stored in FIFO8 to generate the FIFO_READY8 interrupt. - The number of data which generates FIFO_READY8 interrupt is (FIFO_READY_SIZE8+1).	0x0000_0000
RSVD0	[15:14]	RW	Reserved	0x0000_0000
SET7	[13:8]	RW	* Select the number of data stored in FIFO7 to generate the FIFO_READY7 interrupt. - The number of data which generates FIFO_READY7 interrupt is (FIFO_READY_SIZE7+1).	0x0000_0000
RSVD1	[7:6]	RW	Reserved	0x0000_0000
SET6	[5:0]	RW	* Select the number of data stored in FIFO6 to generate the FIFO_READY6 interrupt. - The number of data which generates FIFO_READY6 interrupt is (FIFO_READY_SIZE6+1).	0x0000_0000

5.2.5.3.1.24 FIFO_DATA_SDC

- Base Address: 0x4001_A000
- Address = Base Address + 0x0560, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
FIFO_DATA_SDC	[4:0]	R	SDC FIFO Read data	0x0000_0000

5.2.5.3.1.25 FIFO_INT_STATUS

- Base Address: 0x4001_A000
- Address = Base Address + 0x0564, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
FIFO_INT_STATUS	[11:0]	R	[0]: Interrupt output for NVIC, [1]: synchronized interrupt output, [2]: Interrupt sourcing oring, [11:3]: Each FIFO's interrupt status	0x0000_0000

5.2.5.3.1.26 SAR_SEL

- Base Address: 0x4001_A000
- Address = Base Address + 0x0600, Reset Value = 0x0002_C688

Name	Bit	Type	Description	Reset Value
ADC2_CH1	[17:15]	RW	3'b0 : ADC0_CH0 3'b1 : ADC0_CH1 3'b2 : ADC1_CH0 3'b3 : ADC1_CH1 3'b4 : ADC2_CH0 3'b5 : ADC2_CH1	0x0000_0005
ADC2_CH0	[14:12]	RW	3'b0 : ADC0_CH0 3'b1 : ADC0_CH1 3'b2 : ADC1_CH0 3'b3 : ADC1_CH1 3'b4 : ADC2_CH0 3'b5 : ADC2_CH1	0x0000_0004
ADC1_CH1	[11:9]	RW	3'b0 : ADC0_CH0 3'b1 : ADC0_CH1 3'b2 : ADC1_CH0 3'b3 : ADC1_CH1 3'b4 : ADC2_CH0 3'b5 : ADC2_CH1	0x0000_0003
ADC1_CH0	[8:6]	RW	3'b0 : ADC0_CH0 3'b1 : ADC0_CH1 3'b2 : ADC1_CH0 3'b3 : ADC1_CH1 3'b4 : ADC2_CH0 3'b5 : ADC2_CH1	0x0000_0002
ADC0_CH1	[5:3]	RW	3'b0 : ADC0_CH0 3'b1 : ADC0_CH1 3'b2 : ADC1_CH0 3'b3 : ADC1_CH1 3'b4 : ADC2_CH0 3'b5 : ADC2_CH1	0x0000_0001
ADC0_CH0	[2:0]	RW	3'b0 : ADC0_CH0 3'b1 : ADC0_CH1 3'b2 : ADC1_CH0 3'b3 : ADC1_CH1 3'b4 : ADC2_CH0 3'b5 : ADC2_CH1	0x0000_0000

5.2.5.3.1.27 DC_COMPEN_ADC0

- Base Address: 0x4001_A000
- Address = Base Address + 0x0604, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CH1	[19:10]	RW	ADC0_CH1	0x0000_0000
CH0	[9:0]	RW	ADC0_CH0	0x0000_0000

5.2.5.3.1.28 DC_COMPEN_ADC1

- Base Address: 0x4001_A000
- Address = Base Address + 0x0608, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CH1	[19:10]	RW	ADC1_CH1	0x0000_0000
CH0	[9:0]	RW	ADC1_CH0	0x0000_0000

5.2.5.3.1.29 DC_COMPEN_ADC2

- Base Address: 0x4001_A000
- Address = Base Address + 0x060C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CH1	[19:10]	RW	ADC2_CH1	0x0000_0000
CH0	[9:0]	RW	ADC2_CH0	0x0000_0000

5.2.5.3.1.30 SAR_ADC0_CH0_DATA

- Base Address: 0x4001_A000
- Address = Base Address + 0x061C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
SAR_ADC0_CH0_DATA	[11:0]	R	Direct read data of ADC0_CH0	0x0000_0000

5.2.5.3.1.31 SAR_ADC0_CH1_DATA

- Base Address: 0x4001_A000
- Address = Base Address + 0x0620, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
SAR_ADC0_CH1_DATA	[11:0]	R	Direct read data of ADC0_CH1	0x0000_0000

5.2.5.3.1.32 SAR_ADC1_CH0_DATA

- Base Address: 0x4001_A000
- Address = Base Address + 0x0624, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
SAR_ADC1_CH0_DATA	[11:0]	R	Direct read data of ADC1_CH0	0x0000_0000

5.2.5.3.1.33 SAR_ADC1_CH1_DATA

- Base Address: 0x4001_A000
- Address = Base Address + 0x0628, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
SAR_ADC1_CH1_DATA	[11:0]	R	Direct read data of ADC1_CH1	0x0000_0000

5.2.5.3.1.34 SAR_ADC2_CH0_DATA

- Base Address: 0x4001_A000
- Address = Base Address + 0x062C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
SAR_ADC2_CH0_DATA	[11:0]	R	Direct read data of ADC2_CH0	0x0000_0000

5.2.5.3.1.35 SAR_ADC2_CH1_DATA

- Base Address: 0x4001_A000
- Address = Base Address + 0x0630, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
SAR_ADC2_CH1_DATA	[11:0]	R	Direct read data of ADC2_CH1	0x0000_0000

5.2.5.3.1.36 SD_ADC0_DATA

- Base Address: 0x4001_A000
- Address = Base Address + 0x0634, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
SD_ADC0_DATA	[23:0]	R	Direct read data of IDC0	0x0000_0000

5.2.5.3.1.37 SD_ADC1_DATA

- Base Address: 0x4001_A000
- Address = Base Address + 0x0638, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
SD_ADC1_DATA	[23:0]	R	Direct read data of IDC1	0x0000_0000

5.2.5.3.1.38 SD_ADC2_DATA

- Base Address: 0x4001_A000
- Address = Base Address + 0x063C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
SD_ADC2_DATA	[23:0]	R	Direct read data of SD_ADC	0x0000_0000

6 Application Circuits

This chapter describes application circuits of S1SBP6A.

This chapter includes the following sections:

- Common application circuit
- Application circuit for ECG
- Application circuit for PPG
- Application circuit for BIA
- Application circuit for GSR

6.1 Common Application Circuit

Figure 6-1 illustrates an application circuit for powers, clocks, and reference of S1SBP6A. All the decoupling capacitors should be as close as possible to the device to filter the noise on supply. Other pins should be isolated from XIN, LXOUT, HXIN, and HXOUT because these pins are related to clock source. Capacitors for 32.768 kHz X-tal should be selected considering parasitic effect of a board.

The common application circuit is required for normal operation of S1SBP6A.

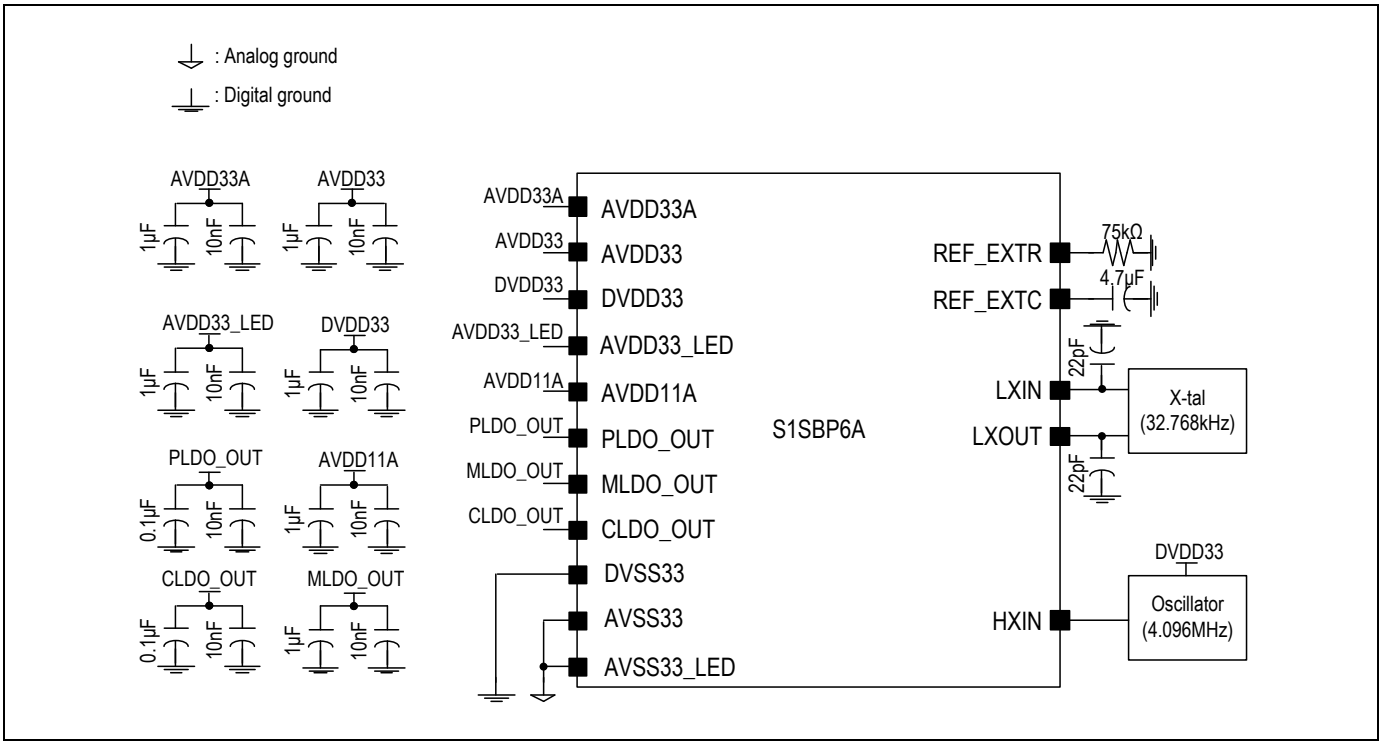


Figure 6-1 Common Application Circuit for S1SBP6A

6.2 Application Circuit for ECG

Figure 6-2 illustrates an application circuit for ECG of S1SBP6A. Three electrodes are required to measure the bio-potentials of human body. Two external 0.1 μF capacitors could effectively reduce the offsets to obtain sufficient dynamic range of ECG.

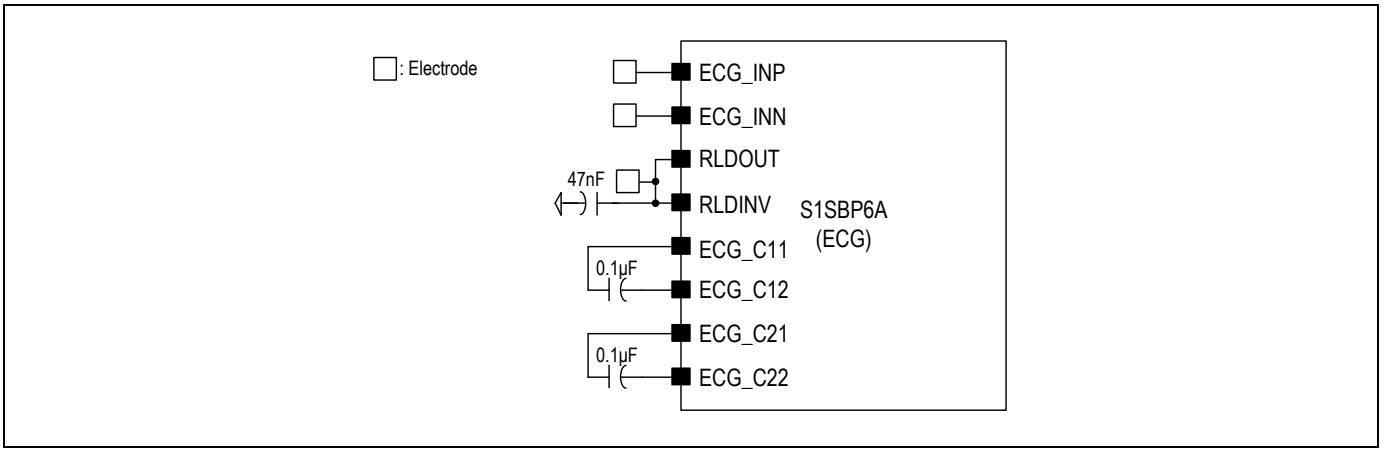


Figure 6-2 Circuit for ECG

6.3 Application Circuit for PPG

Figure 6-3 illustrates a typical connection for the PPG measurement using S1SBP6A. The supply voltage for LEDs can be up to 5 V for LED0 and LED1, and 3 V for LED2 and LED3. PPG_SHIELD shields the PCB patterns for the PPG inputs to minimize the potential capacitive leakage. 4.7 μF and 10 μF capacitors are recommended to filter out excessive noise for the DCC circuit and regulator in IDC respectively.

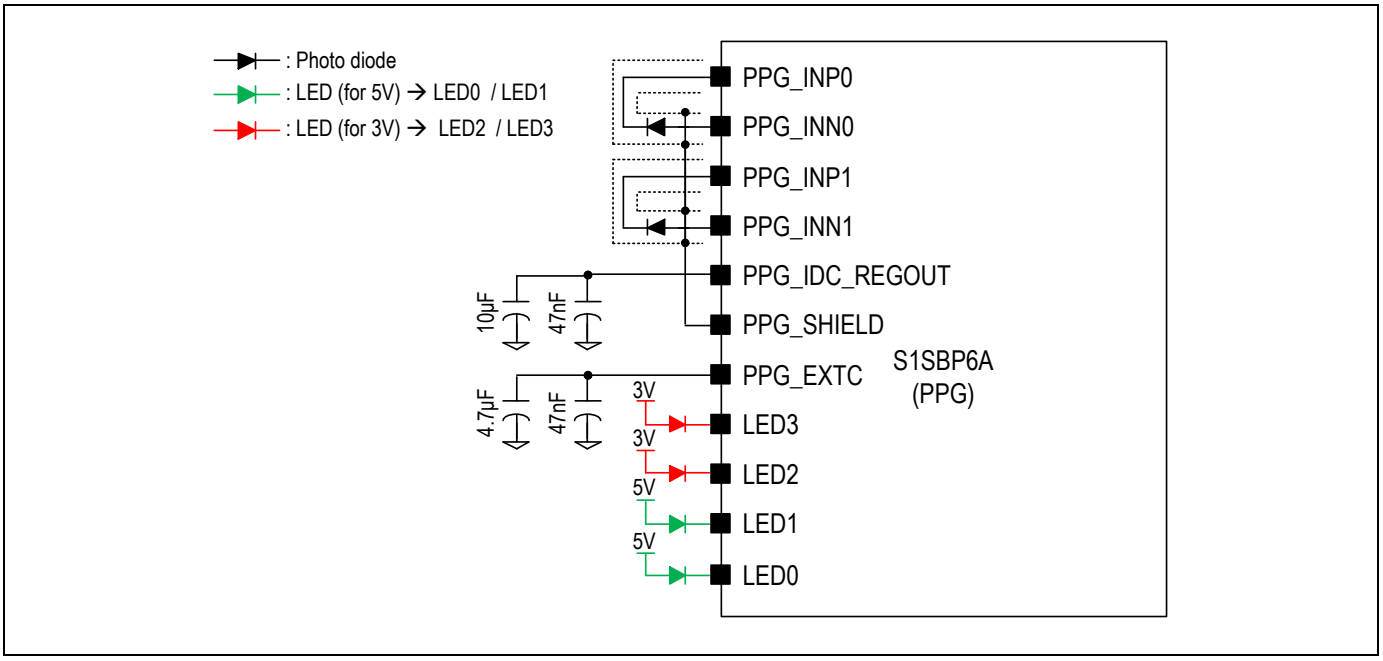


Figure 6-3 Circuit for PPG

6.4 Application Circuit for BIA

Figure 6-4 illustrates an application circuit for BIA of S1SBP6A. When measuring bio-impedance, it needs four electrodes. All the left side components should be of the same pattern to a greater extent.

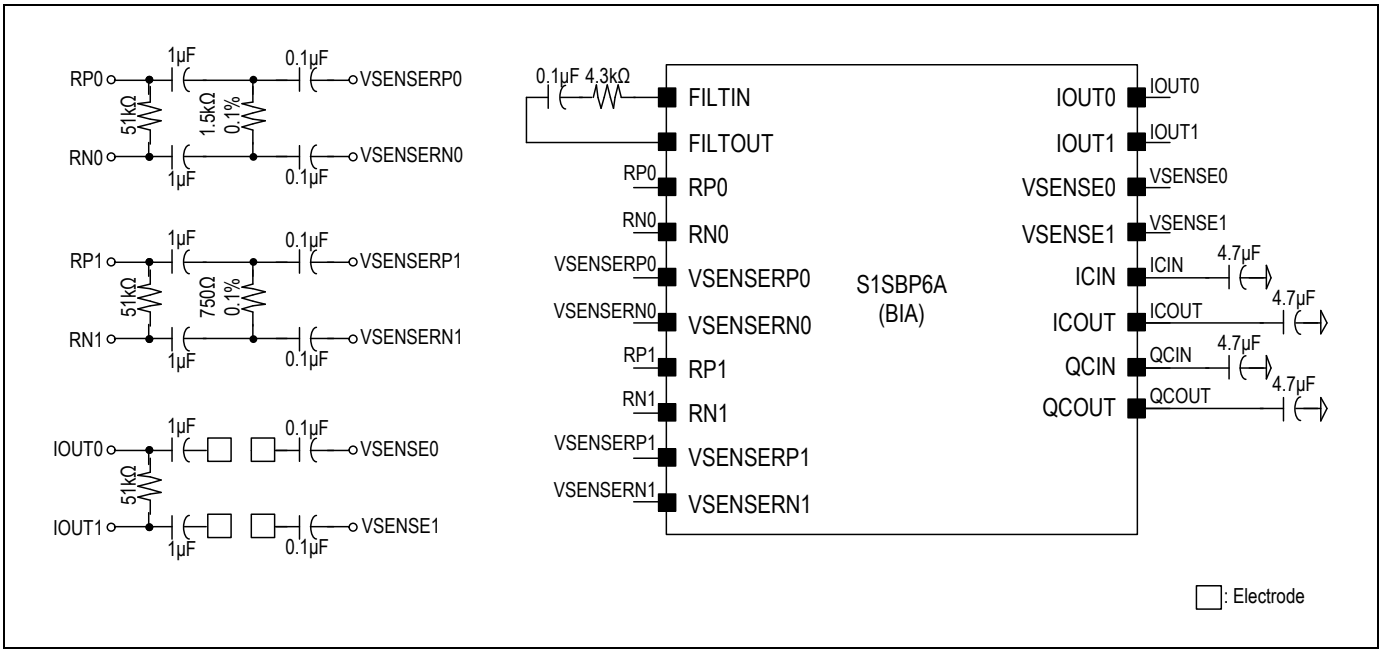


Figure 6-4 Circuit for BIA

7 Reference Schematics and BOM

This chapter includes the following sections:

- Schematics
- Bill of Materials

7.1 Schematics

Figure 7-1 illustrates the top schematic of S1SBP6A.

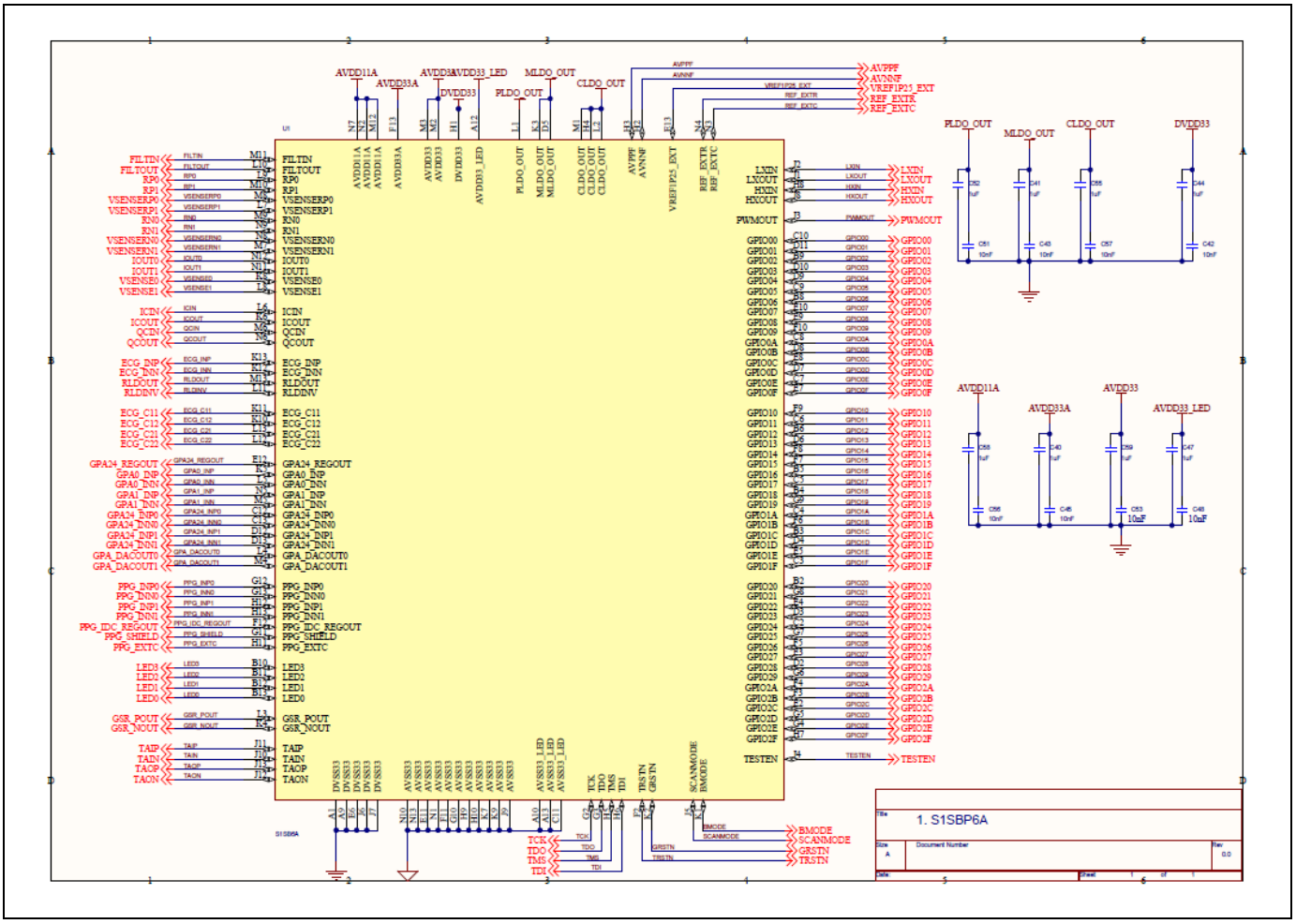


Figure 7-1 Top Schematic of S1SBP6A

Figure 7-2 illustrates the schematic of locks and controls.

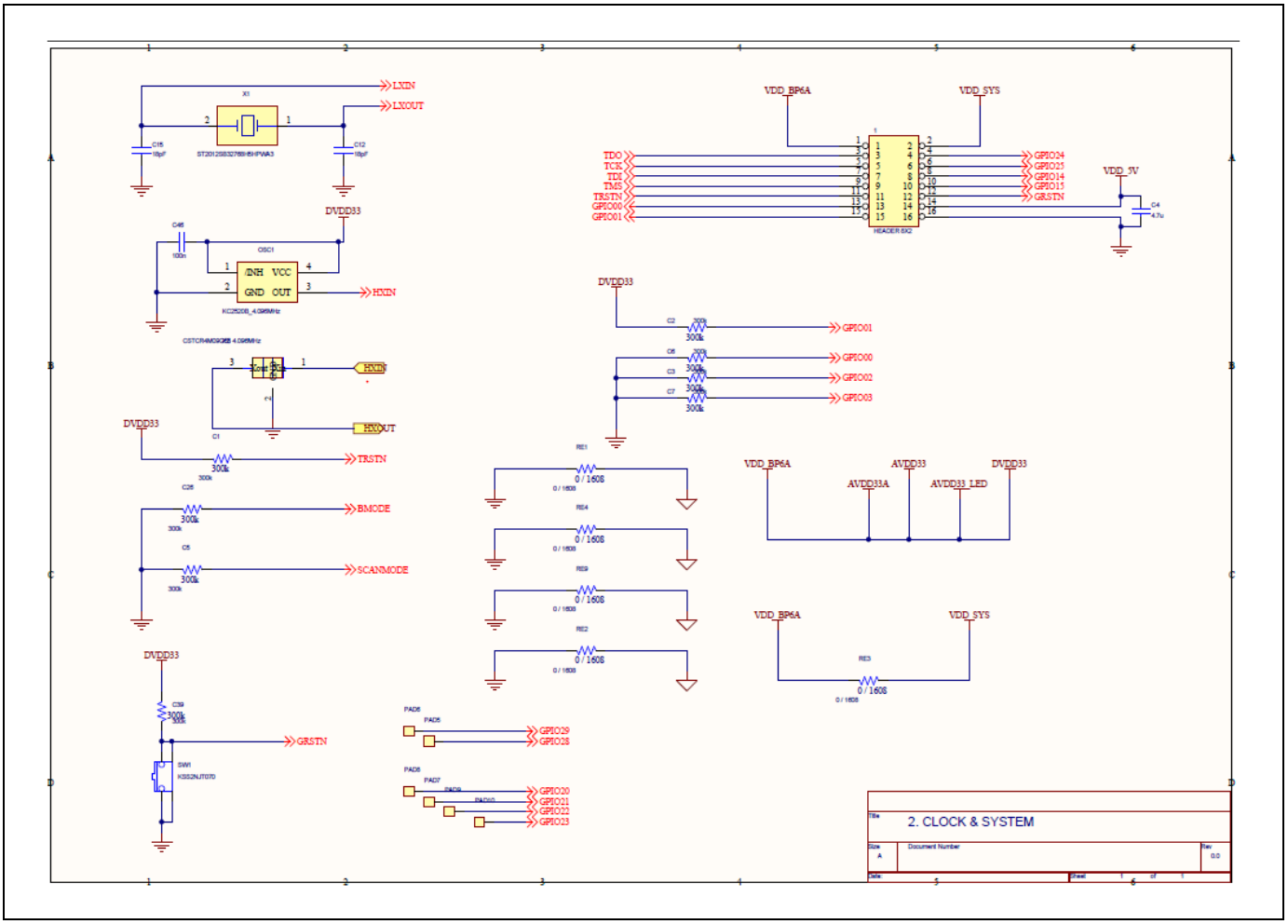


Figure 7-2 Schematic of Clocks and Controls

Figure 7-3 illustrates the schematic of applications.

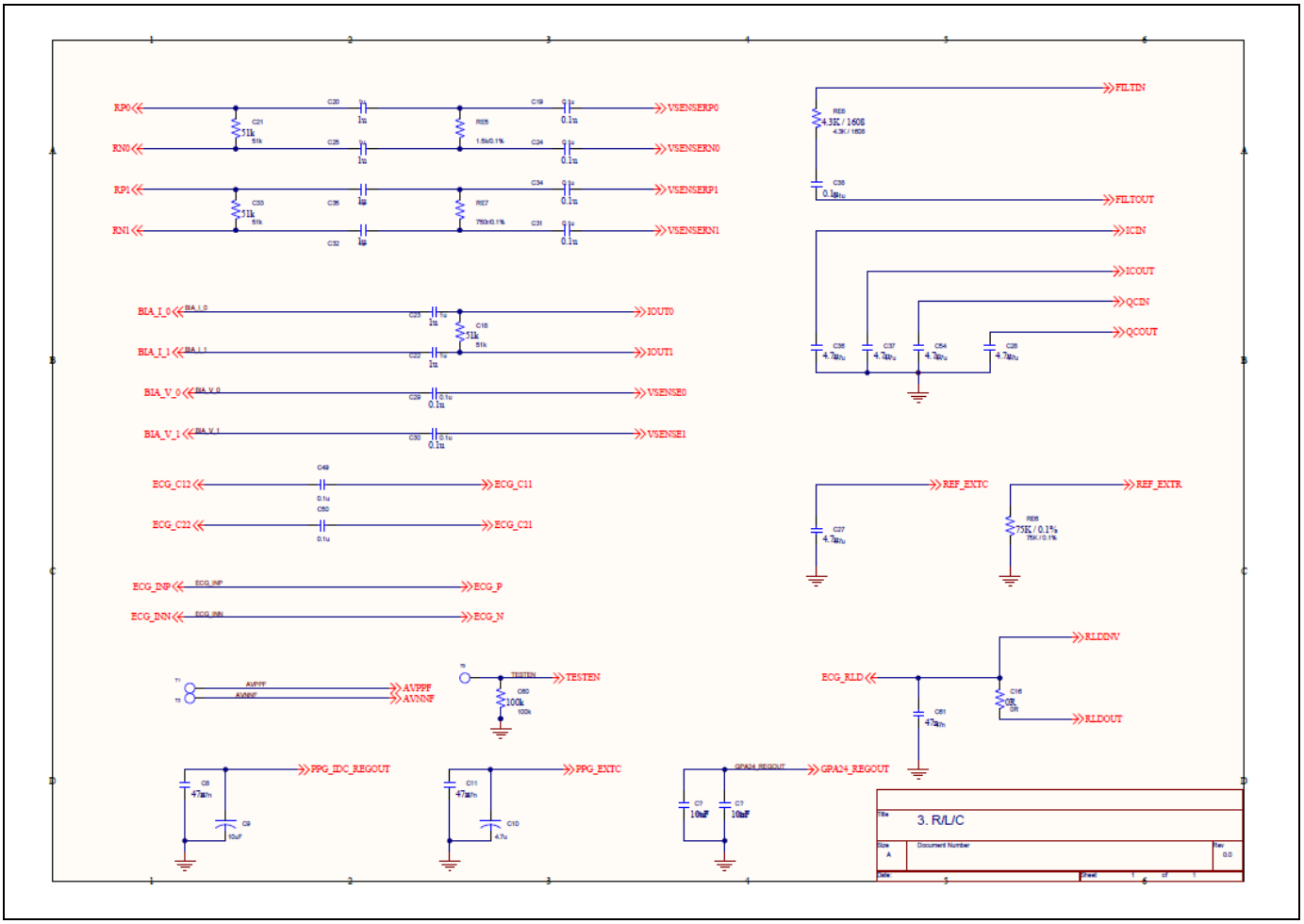


Figure 7-3 Schematic of Applications

7.2 Bill of Materials

Table 7-1 describes the bill of materials.

Table 7-1 Bill of Materials

Item	Description	Value	Quantity	REF.
1	BP6A	DUT	1	U1
2	Ceramic Capacitor (optional)	10 nF	9	C13, C42, C43, C45, C48, C51, C53, C56, C57
3	Ceramic Capacitor	0.1 μF	9	C19, C24, C29, C30, C31, C34, C38, C49, C50
4	Ceramic Capacitor	1 μF	14	C40, C41, C44, C47, C52, C55, C58, C59, C20, C22, C23, C25, C32, C35
5	Ceramic Capacitor	10 μF	2	C9, C14
6	Ceramic Capacitor (optional)	47 nF	2	C8, C11
7	Ceramic Capacitor	47 nF	1	C61
8	Ceramic Capacitor	4.7 μF	7	C4, C10, C27, C28, C36, C37, C54
9	Ceramic Capacitor	100 nF	1	C46
10	Ceramic Capacitor	22 pF (can be changed considering board parasitics)	2	C12, C15
11	Resistor	100 kΩ	1	C60
12	Resistor	300 kΩ	8	C1, C2, C3, C5, C6, C7, C26, C39
13	Resistor	51 kΩ	3	C18, C21, C33
14	Resistor (optional)	0 Ω	1	C16
15	Resistor	1500 Ω / 0.1%	1	RE5
16	Resistor	750 Ω / 0.1%	1	RE7
17	Resistor	75 kΩ / 0.1%	1	RE6
18	Resistor	4.3 kΩ	1	RE8
19	Resistor (optional)	0 Ω	5	RE1, RE2, RE3, RE4, RE9
20	No Connection (optional)	CSTCR4M09G55	1	X2
21	CRYSTAL	ST2012SB32768H5HPWA3	1	X1
22	Oscillator	KC2520B_4.096 MHz	1	OSC1
23	Switch (optional)	KSS2NJT070	1	SW1

8 Mechanical Data

Figure 8-1 illustrates the 154 pin WLP outline.

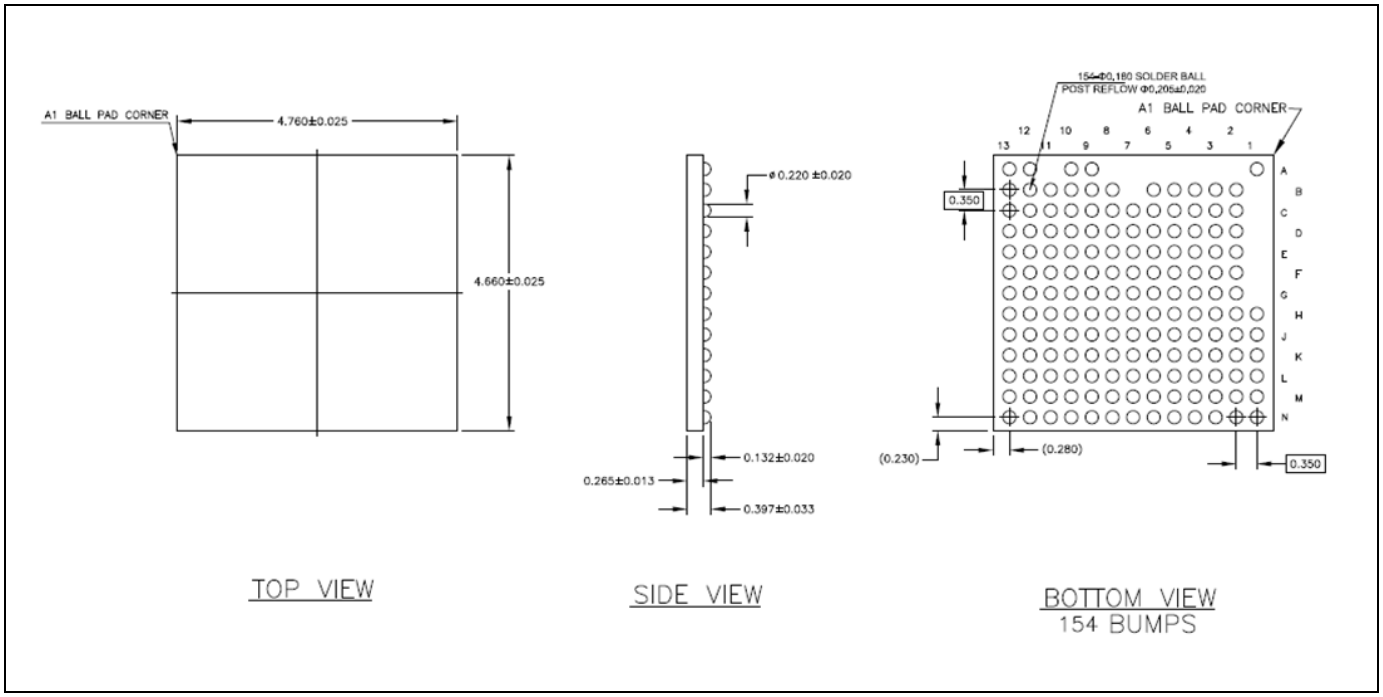


Figure 8-1 154 Pin WLP (4.76 × 4.66 × 0.43 mm) Outline