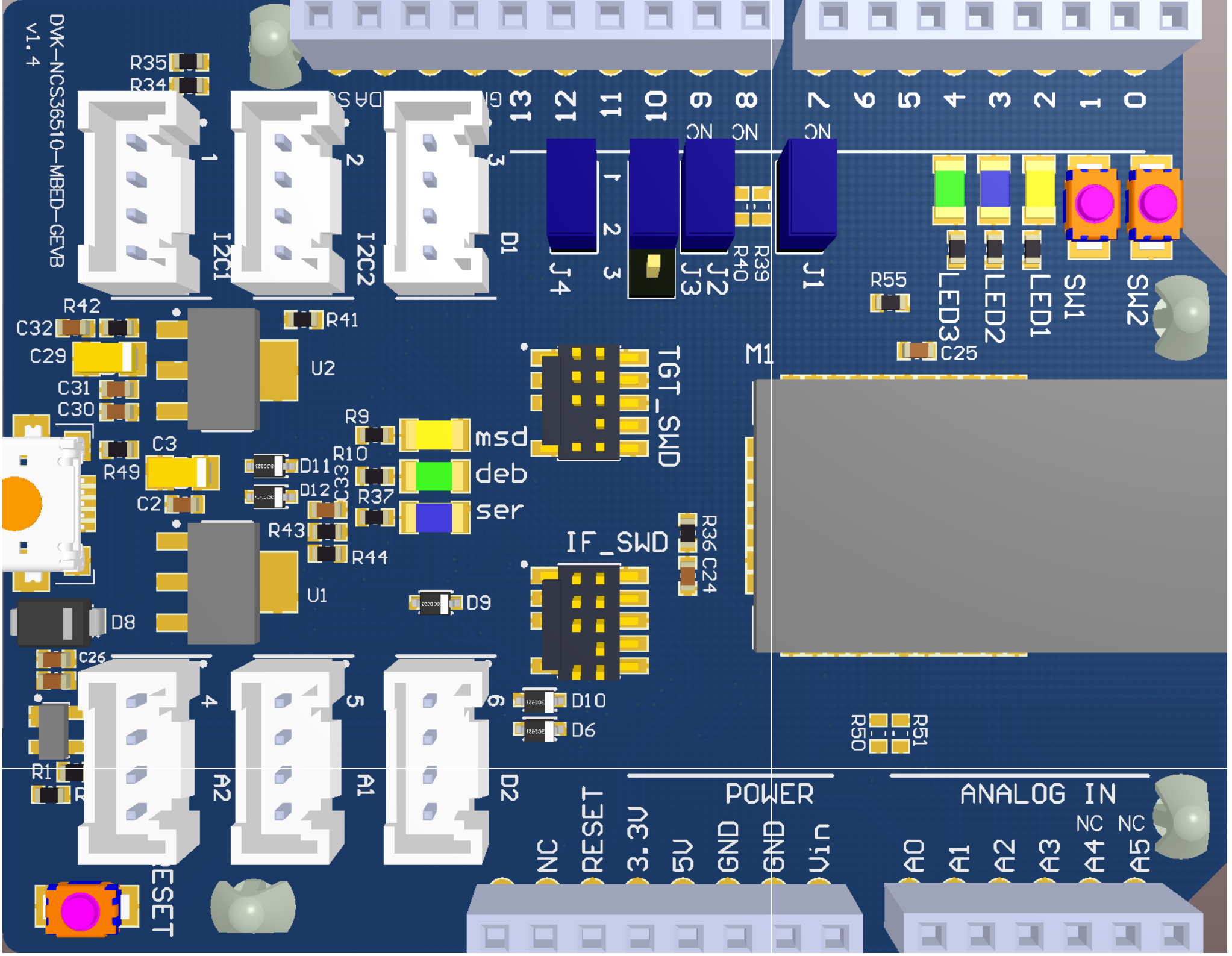


DVK-NCS36510-MBED-GEVB
V1.4



RESET

ANALOG IN
A0 A1 A2 A3 A4 A5
NC NC

POWER
DNG DNG U1IN

RESET
3-3 NC

D2 D10 D6
A1 A2
4 5 6

MSD
DEB
SER

IF_SWD

TGT_SWD

DAS
I2C1 I2C2 I2C3
1 2 3

SM1 SM2
LED1 LED2 LED3
0 1 2 3 4 5 6 7 8 9
NC NC

R50 R51

R36 C24

D9

R10 R37 R43 R44

D11 D12

C2 C3

D8

R34 R35

R55

R42 C29 C30 C31 C32

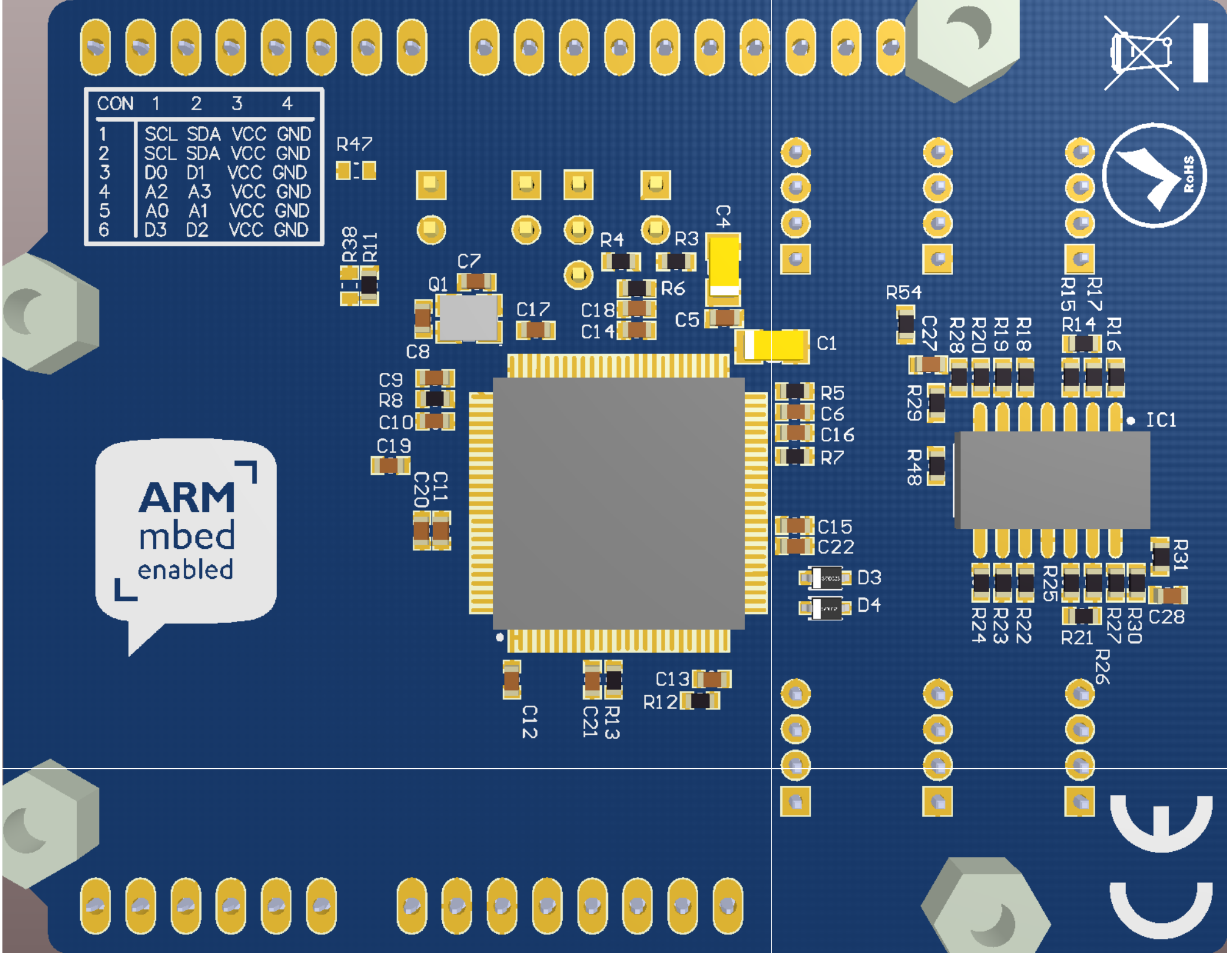
R41

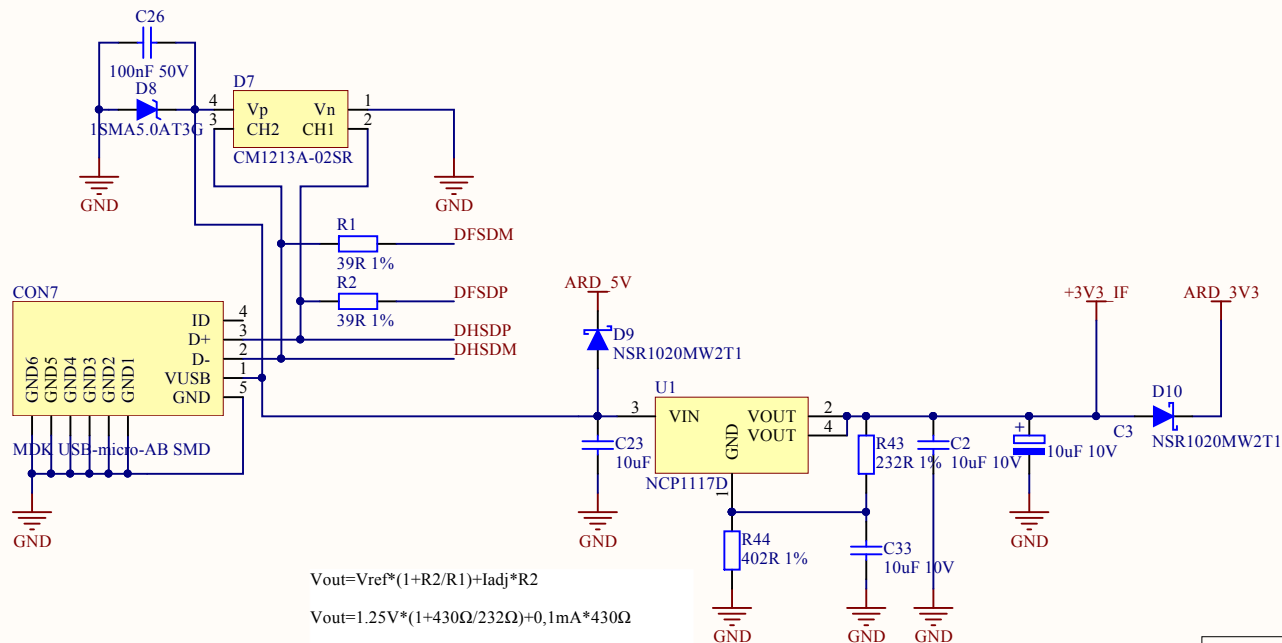
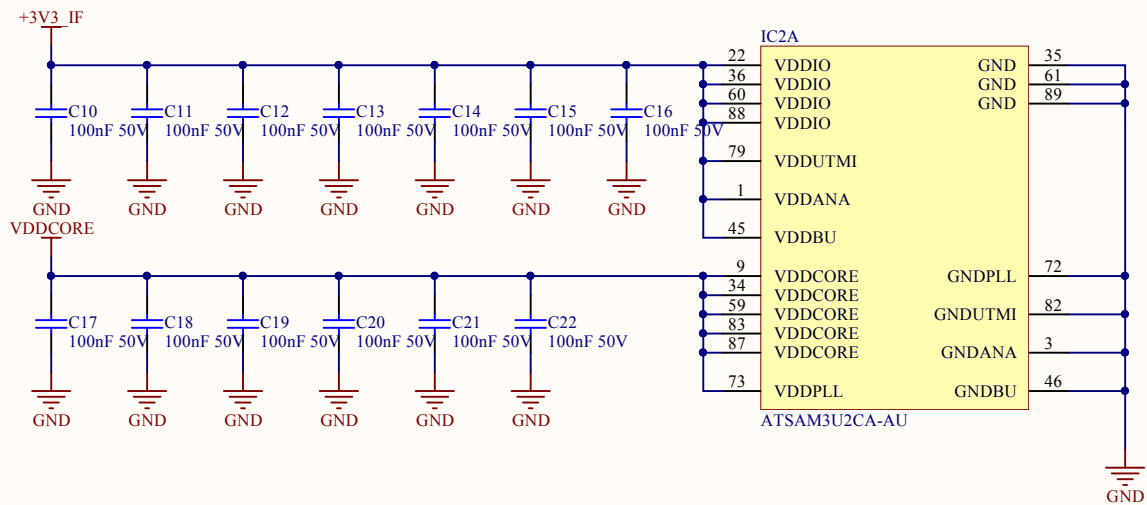
U2

U1

CON	1	2	3	4
1	SCL	SDA	VCC	GND
2	SCL	SDA	VCC	GND
3	D0	D1	VCC	GND
4	A2	A3	VCC	GND
5	A0	A1	VCC	GND
6	D3	D2	VCC	GND

ARM
mbed
enabled





$$V_{out} = V_{ref} * (1 + R2/R1) + I_{adj} * R2$$

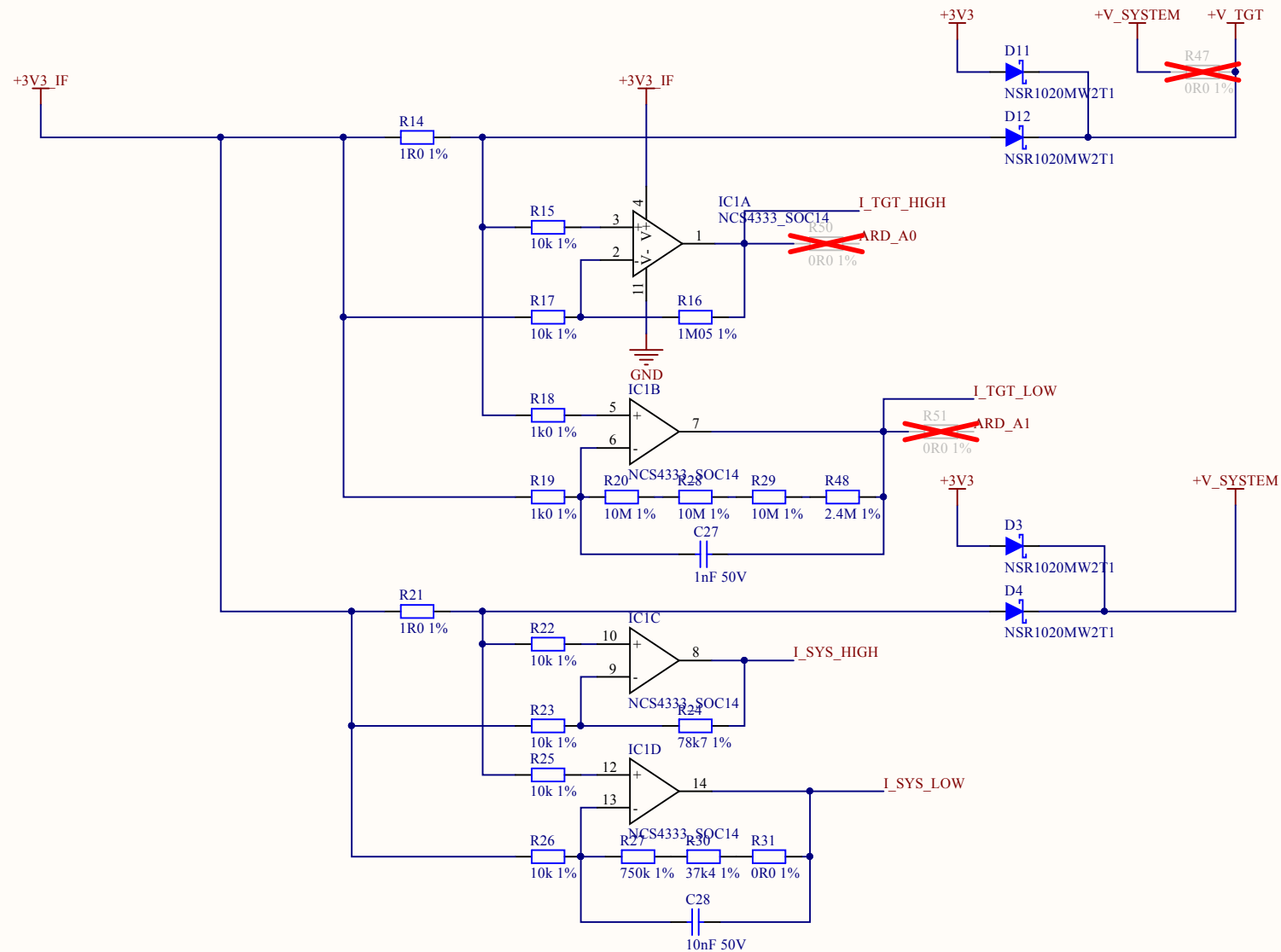
$$V_{out} = 1.25V * (1 + 430\Omega / 232\Omega) + 0,1mA * 430\Omega$$

$$V_{out} = 3.6V$$

DVK-NCS36510-MBED-GEVB

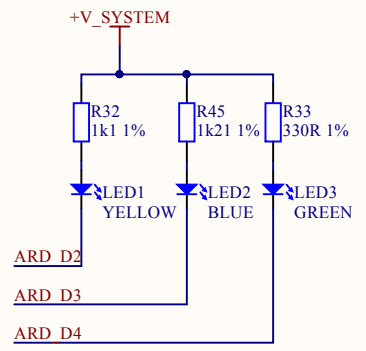
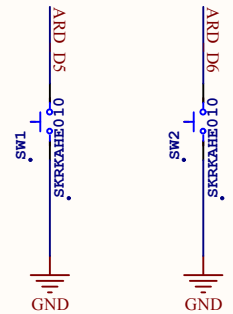
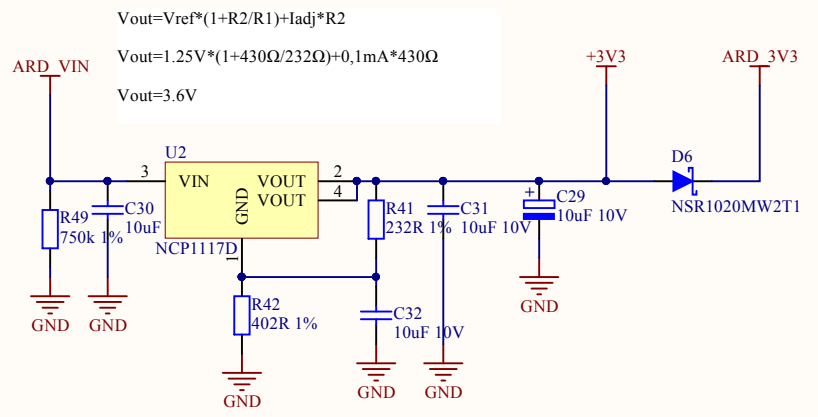
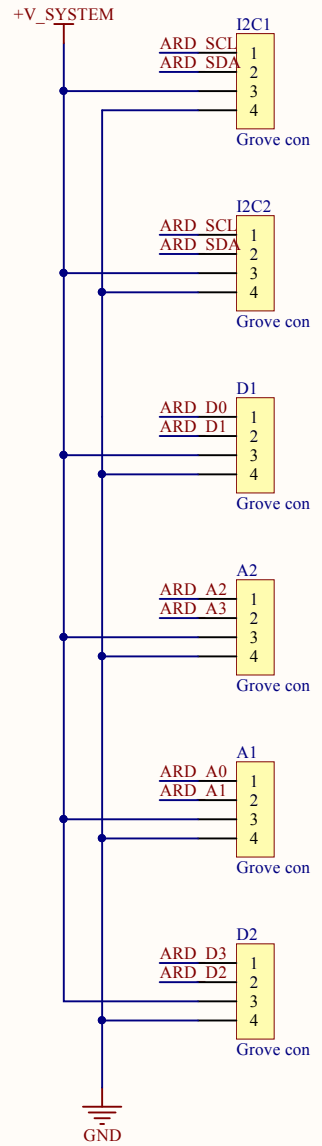
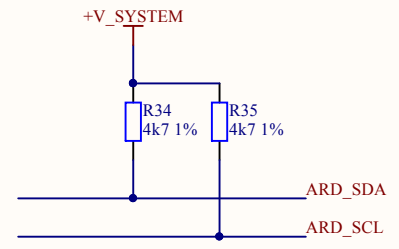
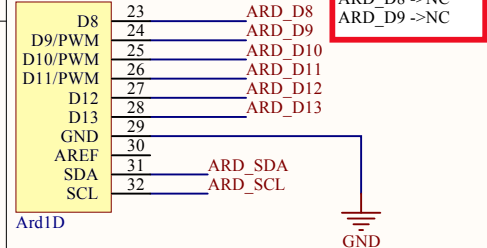
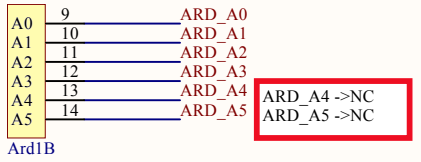
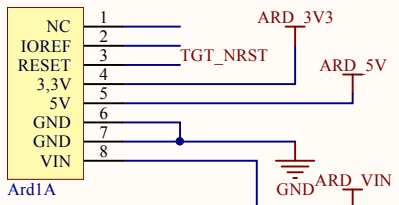
Power.SchDoc	Revision: 1.4
Drawn By: Matej Slapšak	Approved By: Dan Clement
Checked By: Rok Sinkovec	Sheet 1 of 4
Date: 10.7.2017	www.ltek.si info@ltek.si





DVK-NCS36510-MBED-GEVB	
amplifier.SchDoc	Revision: 1.4
Drawn By: Matej Slapšak	Approved By: Dan Clement
Checked By: Rok Sinkovec	Sheet 2 of 4
Date: 10.7.2017	www.ltek.si info@ltek.si



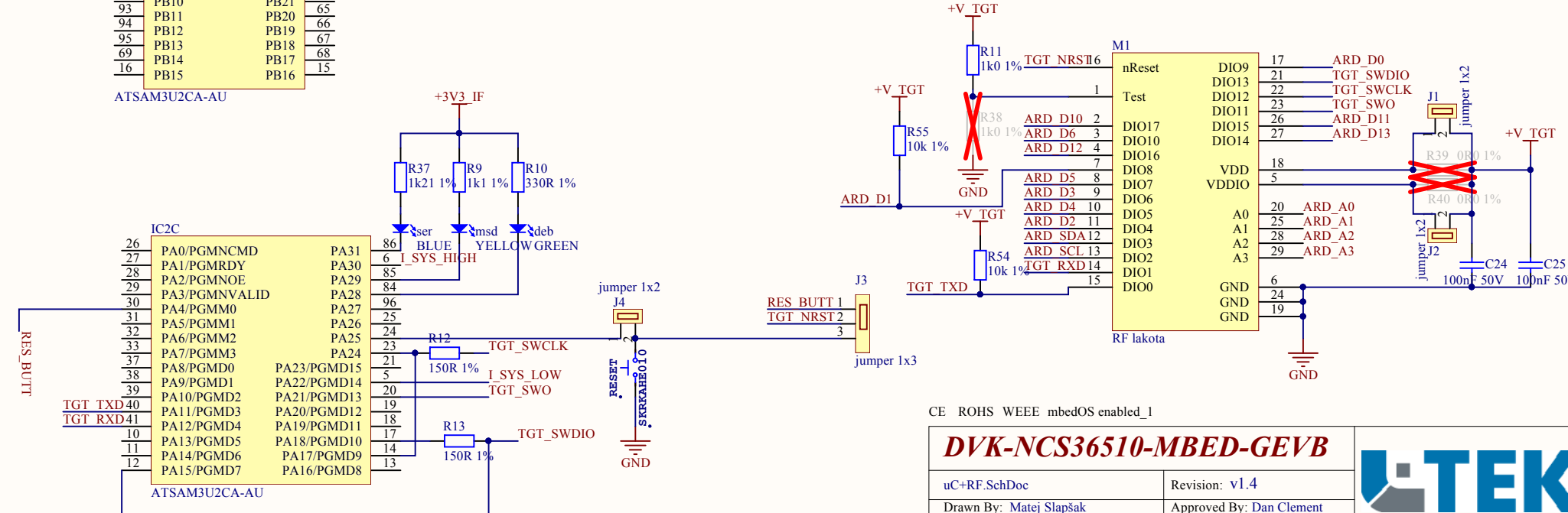
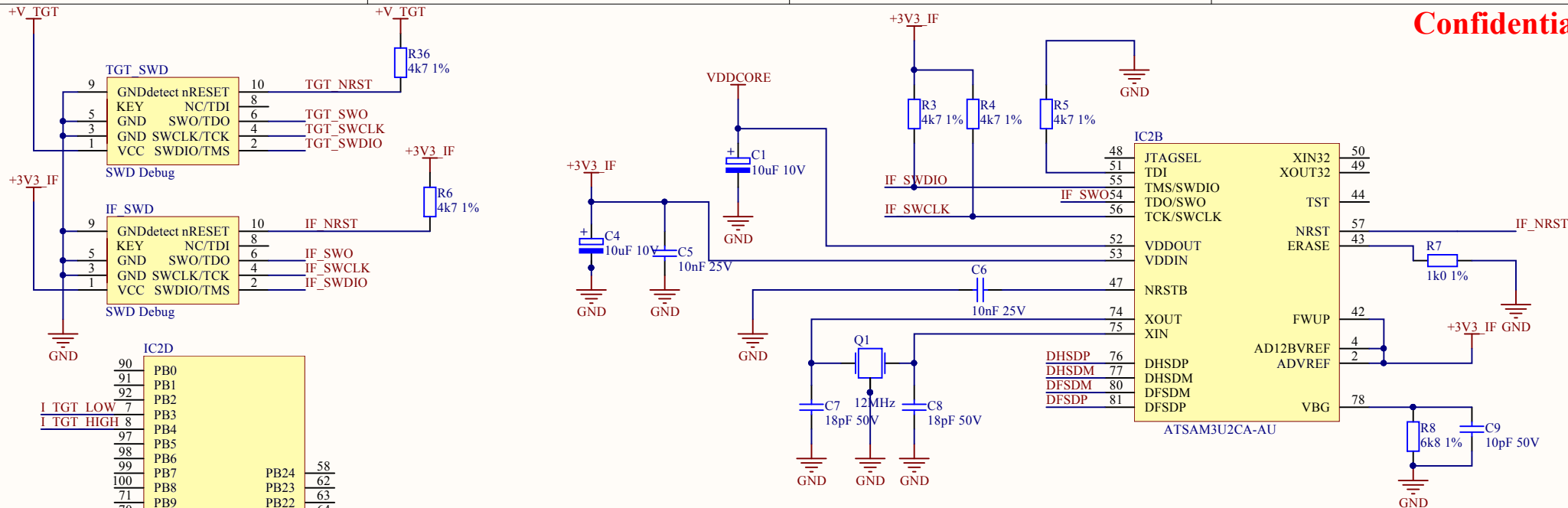


- MEH1
- DURATOOL D01463 PCB SPACER SUPPORT
- MEH2
- DURATOOL D01463 PCB SPACER SUPPORT
- MEH3
- DURATOOL D01463 PCB SPACER SUPPORT
- MEH4
- DURATOOL D01463 PCB SPACER SUPPORT

DVK-NCS36510-MBED-GEVB

grove+arduino_header.SchDoc	Revision: 1.4
Drawn By: Matej Slapšak	Approved By: Dan Clement
Checked By: Rok Sinkovec	Sheet 3 of 4
Date: 10.7.2017	www.ltek.si info@ltek.si

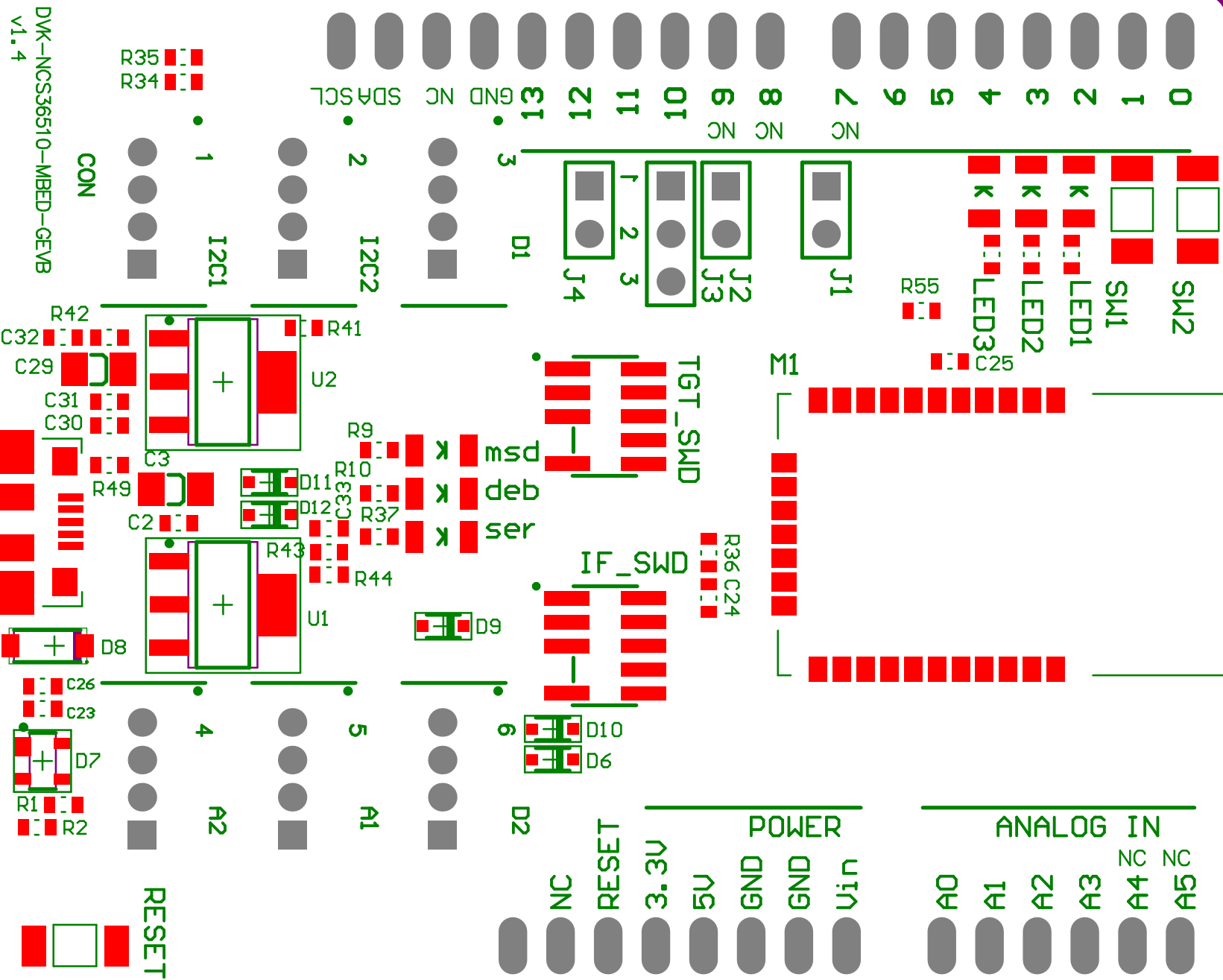




CE ROHS WEEE mbedOS enabled_1

DVK-NCS36510-MBED-GEVB	
uC+RF.SchDoc	Revision: v1.4
Drawn By: Matej Slapšak	Approved By: Dan Clement
Checked By: Rok Šinkovec	Sheet 4 of 4
Date: 10.7.2017	www.ltek.si info@ltek.si





DWK-NCS36510-MBED-GEVB
v1.4

R35
R34

0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

NC
NC
NC
NC
NC
NC
NC
NC
NC
NC
GND
GND
NC
NC
SDA
SCL

SW2
SW1
LED1
LED2
LED3

J1
J2
J3
J4

1
2
3
4
5

I2C1
I2C2

+

U2

+

U1

TGT_SWD

IF_SWD

R42
C29
C31
C30
C3
R49
C2
D8

R41
R9
R10
R37
R44
R43

msd
deb
ser

C26
C23
D7
R1
R2

D9
D10
D6

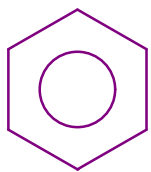
RESET

D2
RESET
3.3V
V5
DNG
DNG
U1V
U1V
ANALOG IN
A0
A1
A2
A3
A4
A5

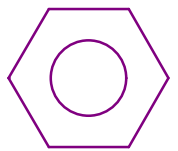
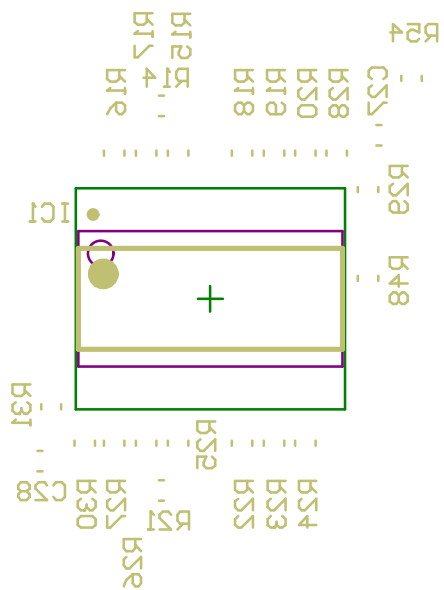
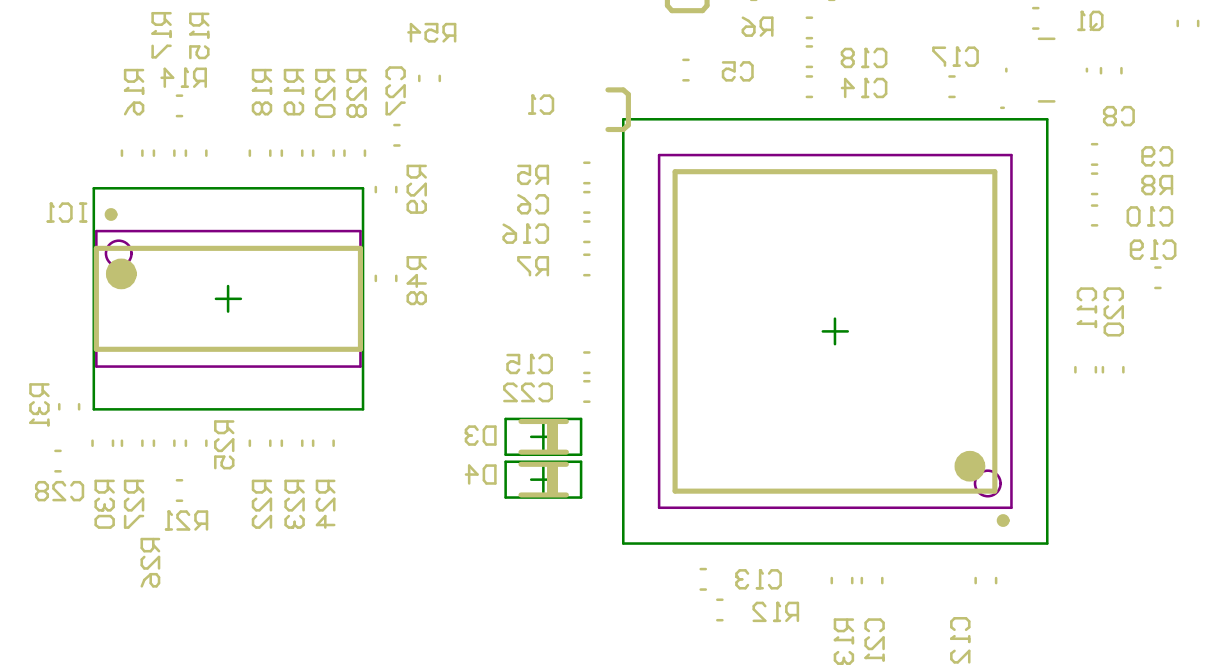
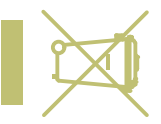
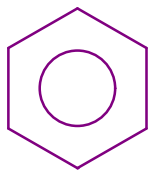
NC
NC
NC
NC
NC
NC



CON	1	2	3	4
1	SCL	SDA	VCC	GND
2	SCL	SDA	VCC	GND
3	DO	D1	VCC	GND
4	A5	A3	VCC	GND
5	A0	A1	VCC	GND
6	D3	D5	VCC	GND

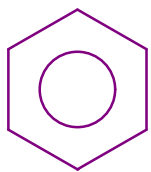


ARM
mped
enabled

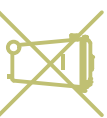
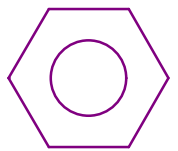
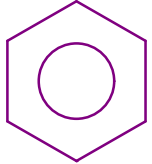
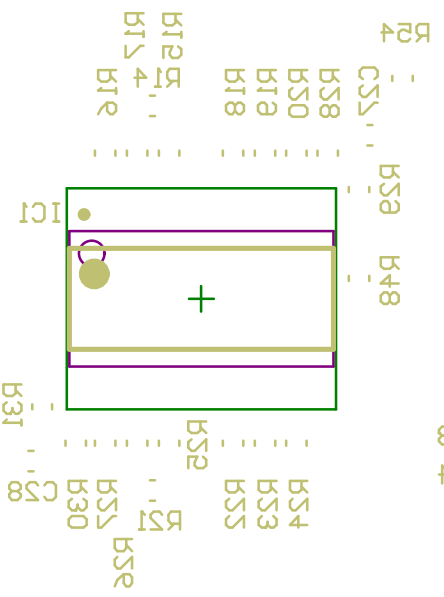
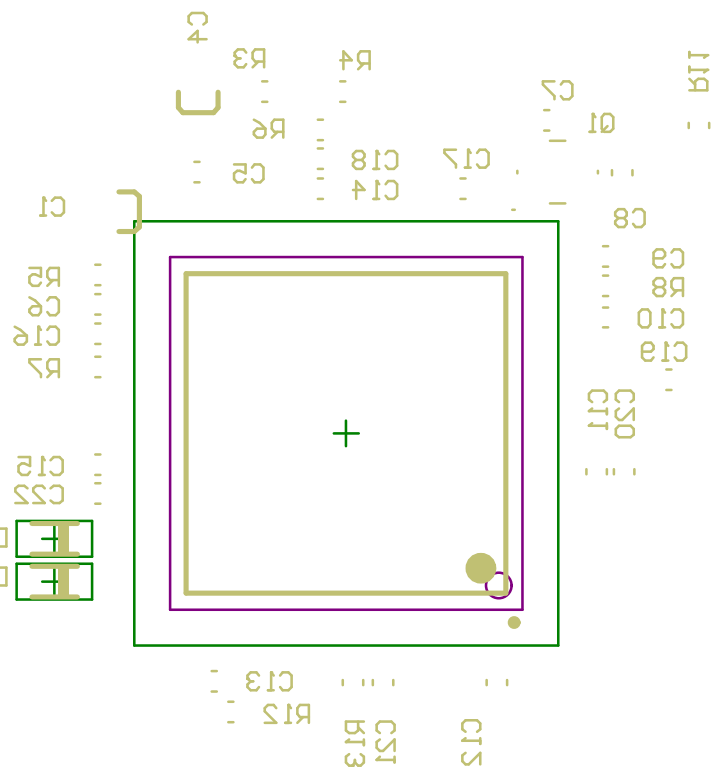
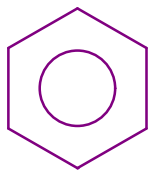


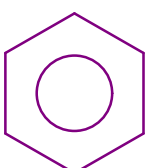
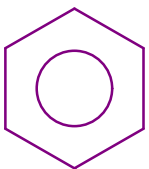


CON	1	2	3	4
1	SCL	SDA	VCC	GND
2	SCL	SDA	VCC	GND
3	DO	D1	VCC	GND
4	A5	A3	VCC	GND
5	A0	A1	VCC	GND
6	D3	D5	VCC	GND



ARM
bed
enabled





ARM
mbed
enabled

CON	1	2	3	4
1	SCL	SDA	VCC	GND
2	SCL	SDA	VCC	GND
3	D0	D1	VCC	GND
4	A5	A3	VCC	GND
5	A0	A1	VCC	GND
6	D3	D5	VCC	GND

